

## PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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Page Description

51	SEQUENCE: MISC
52	LED & FAN HEADERS
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base on V372-02S change for D18 Z  
1. P.23 remove SLI & BRIDGE\_LED\_VDD & SLI\_BRG\_PRST\*  
2. P.52 remove LED change FAN connector  
3. P.53 remove LED  
4. P.38/44 add FUSE  
5. P.5~14 mem add <->  
6. P.53 LED use V336-0D  
7. P.32 remove  
8. P.35~38 dual MOS  
9. P.33 change dual MOS  
10. P.43 remove  
11. P.31 change to UP1666  
12. P.21 remove colay DP

0727:

page 24: REMOVE GPIO29\_IDLE\_IN\_SW  
remove GPIO9\_INPUT\_DYN\_BAL2  
page 29: 12V\_F RTD3 change to 12V\_F  
page 30: 12V\_F RTD3 change to 12V\_F  
page 33: 12V\_F RTD3 change to 12V\_F  
移除保護線路  
page 39: remove INPUT SWITCH RTD3  
page 40: remove INPUT SWITCH RTD3 USB  
page 44: remove INA3221

page 46: remove PFM\_SKIP net  
remove PS\_RTD3\_12V\_SW net  
page 47: remove PS\_VMON\_PGOOD net  
12V\_F RTD3 change to 12V\_F  
remove 3V3\_PORT  
remove 3V3\_RTD3 change to nv3v3  
page 48: remove OC\_CRIT\* NET from ina3221  
remove PS\_VMON\_PGOOD net  
page 49: PCIE Voltage Monitor1  
page 52: REMOVE VIN =>12V\_PEX6\_8\_IN\_OVRS

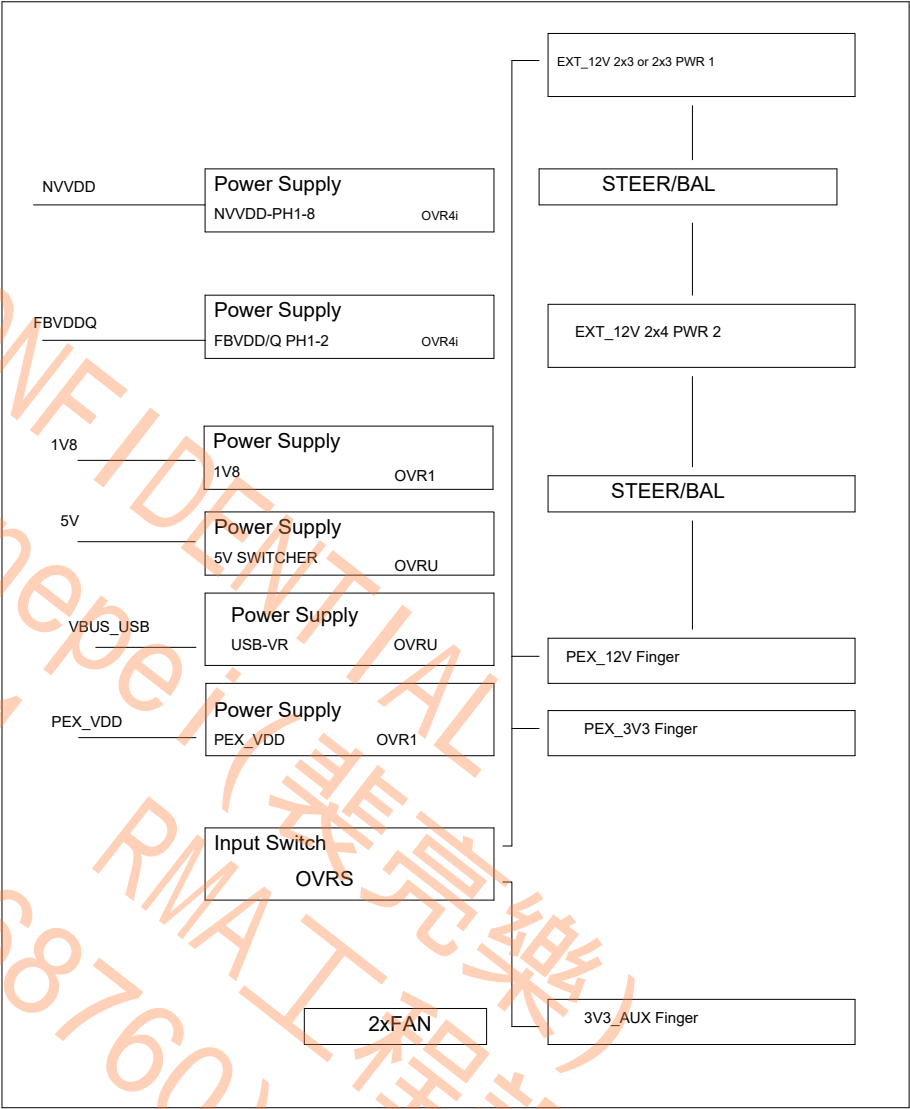
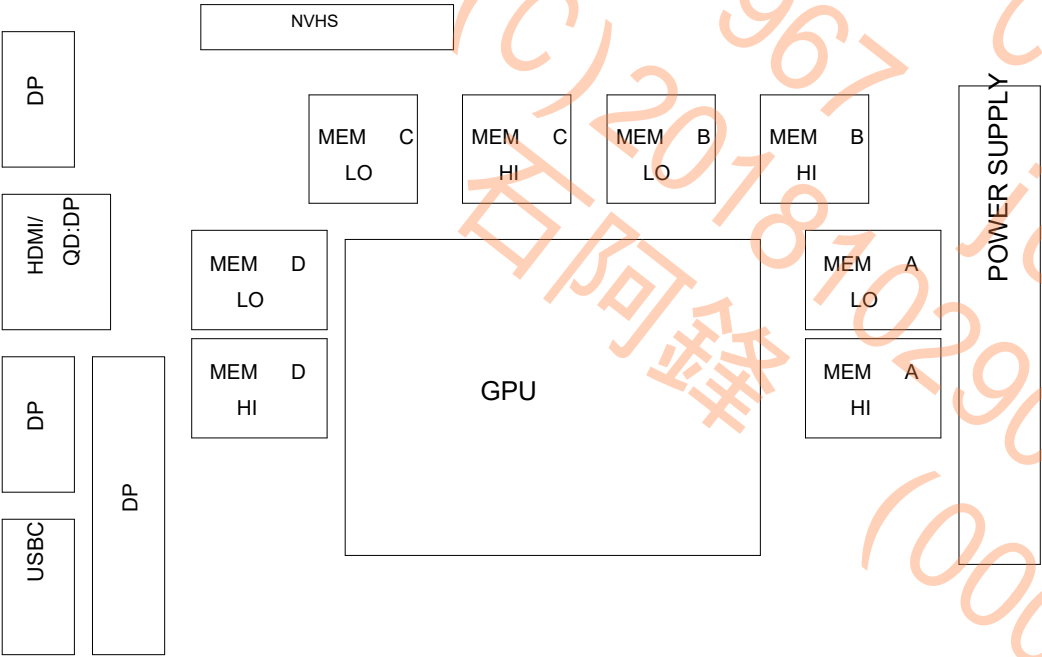
page 54: change GPU screw holes to small size



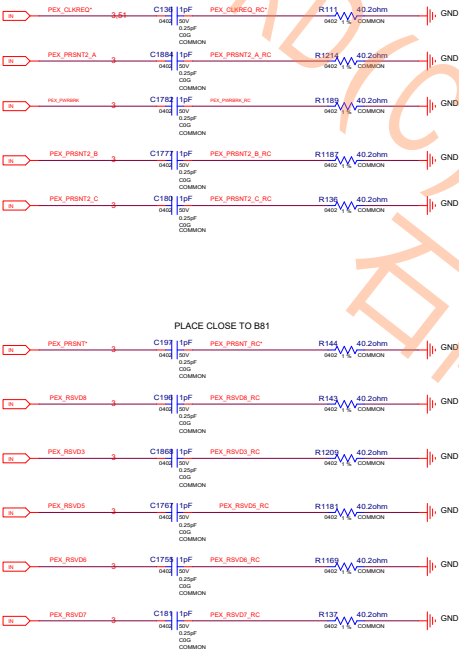
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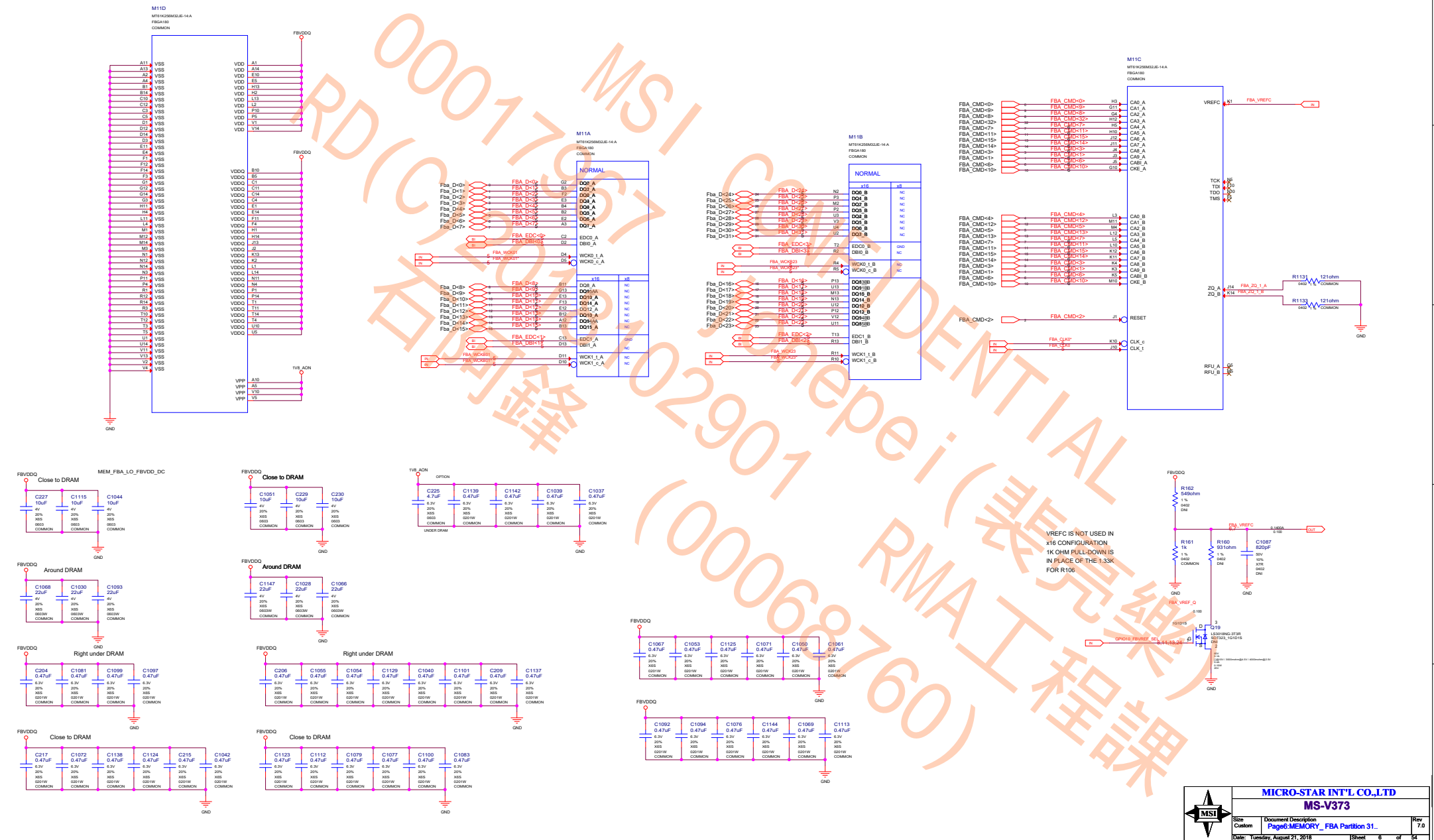
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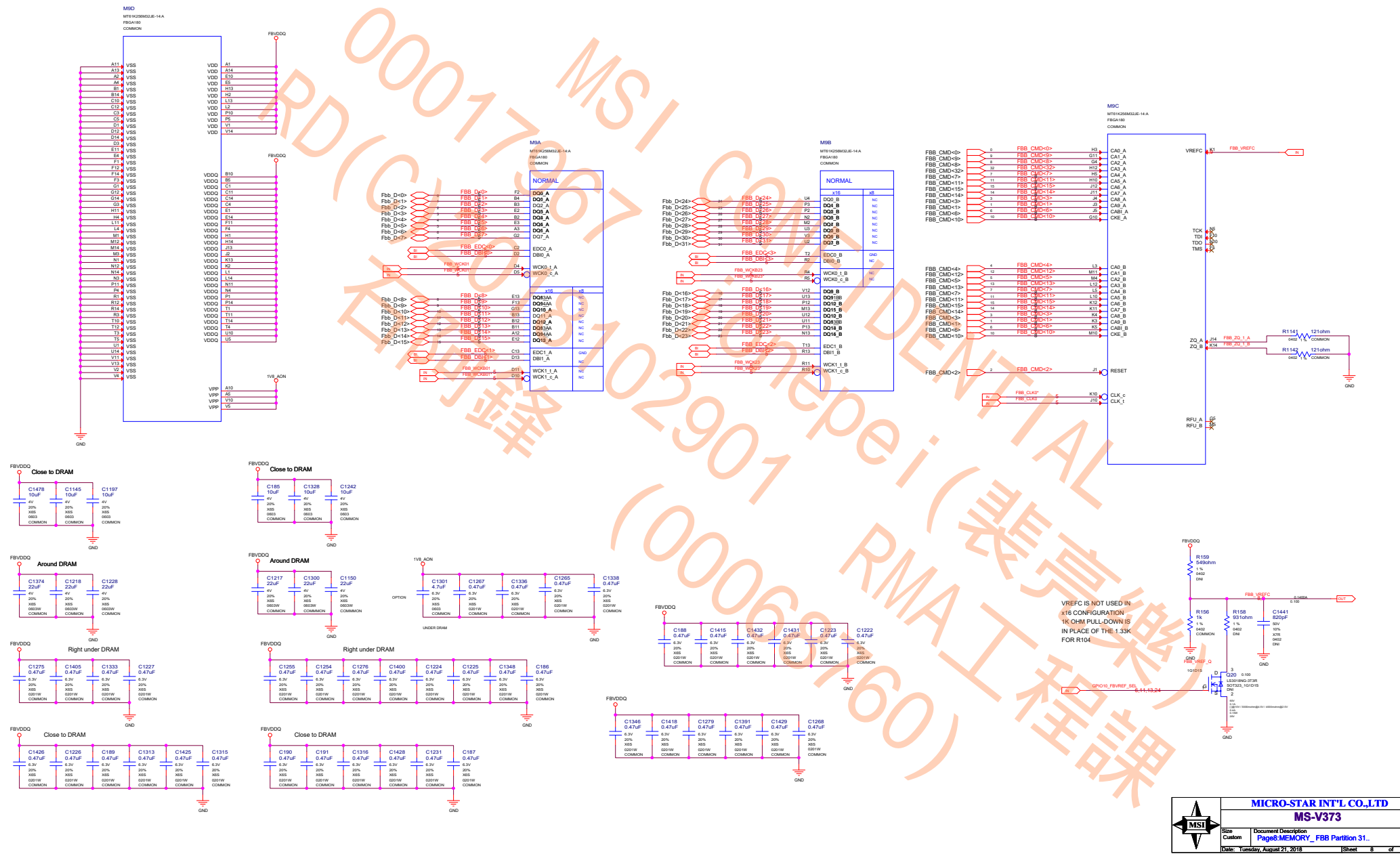








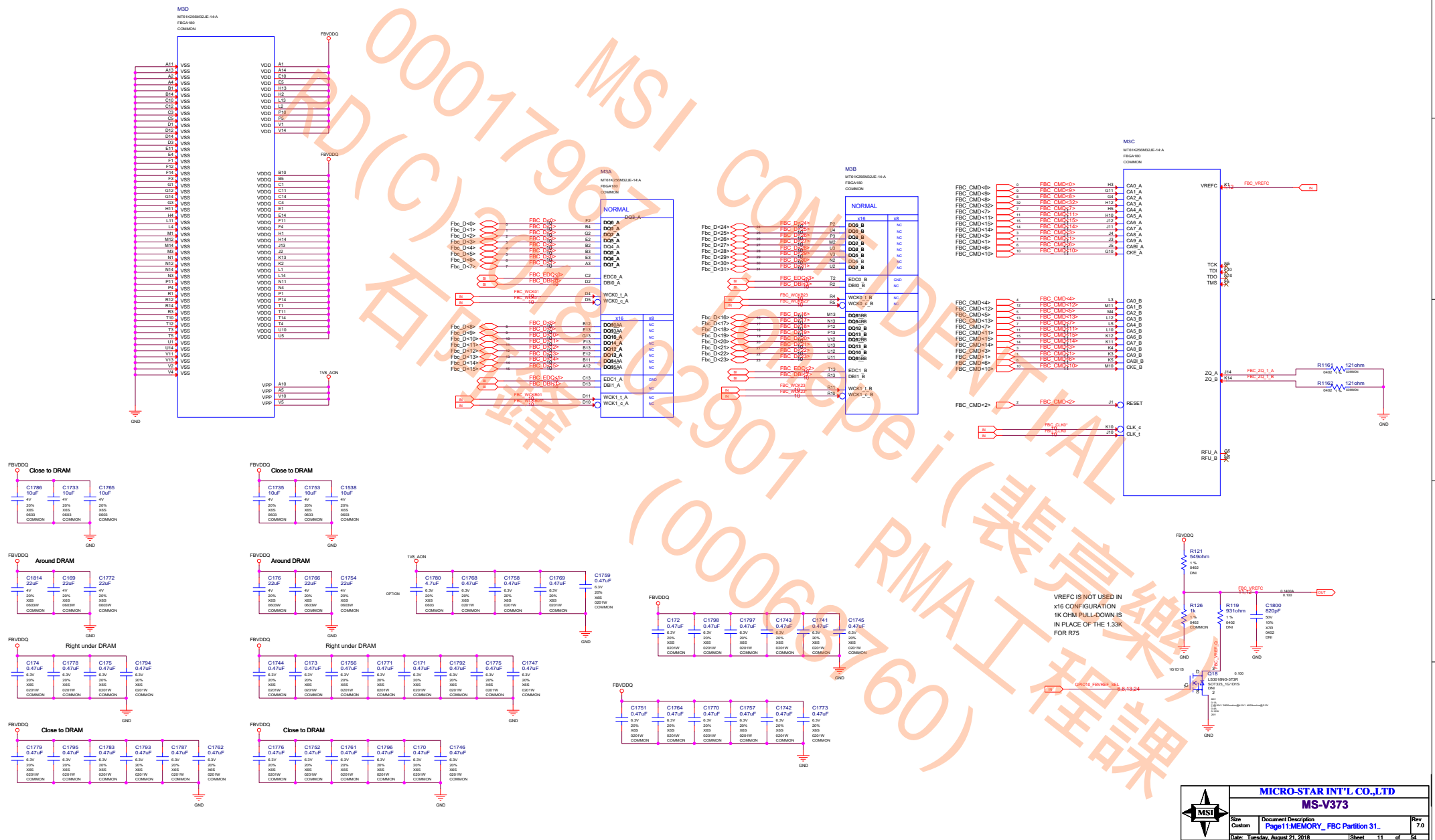


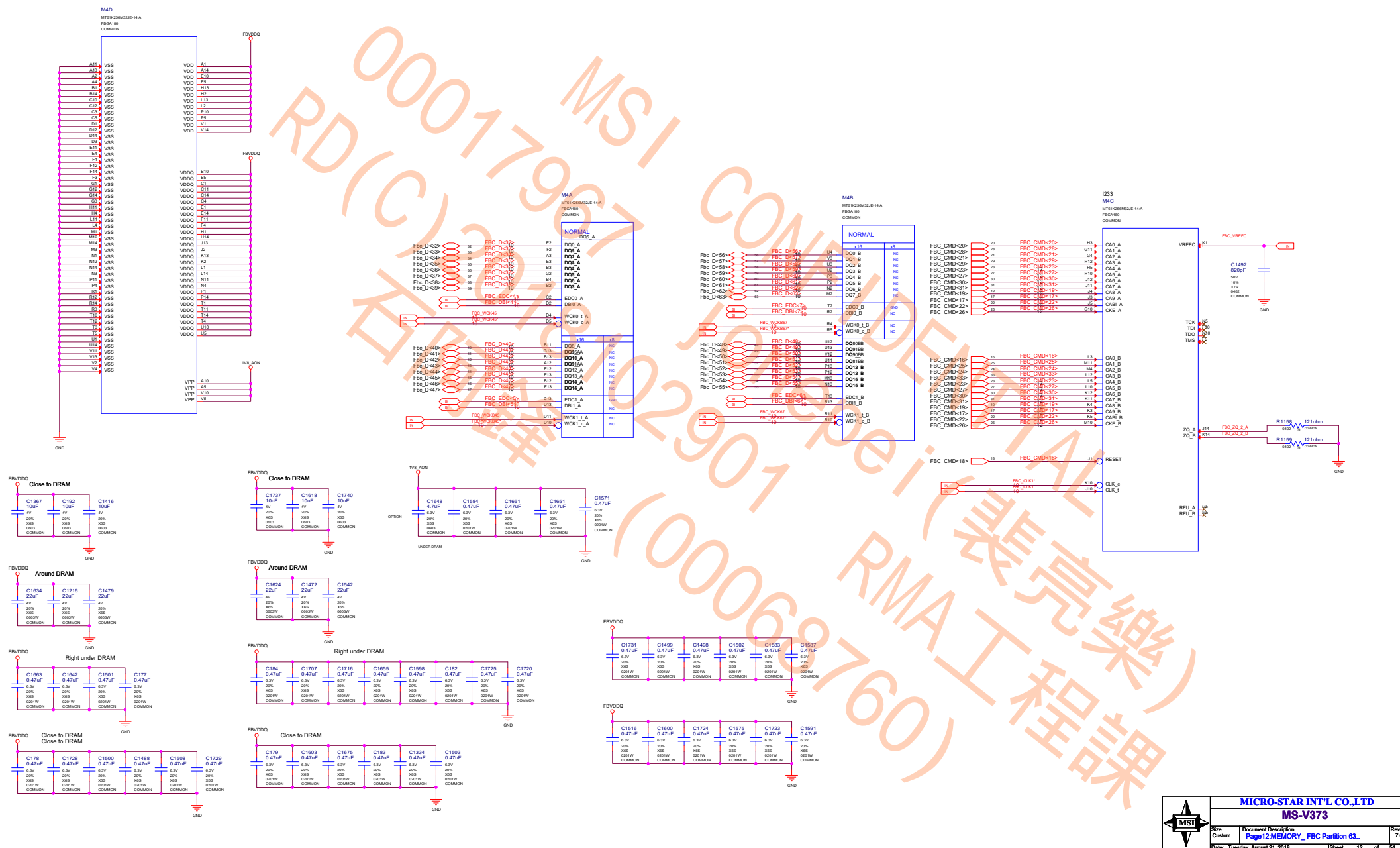




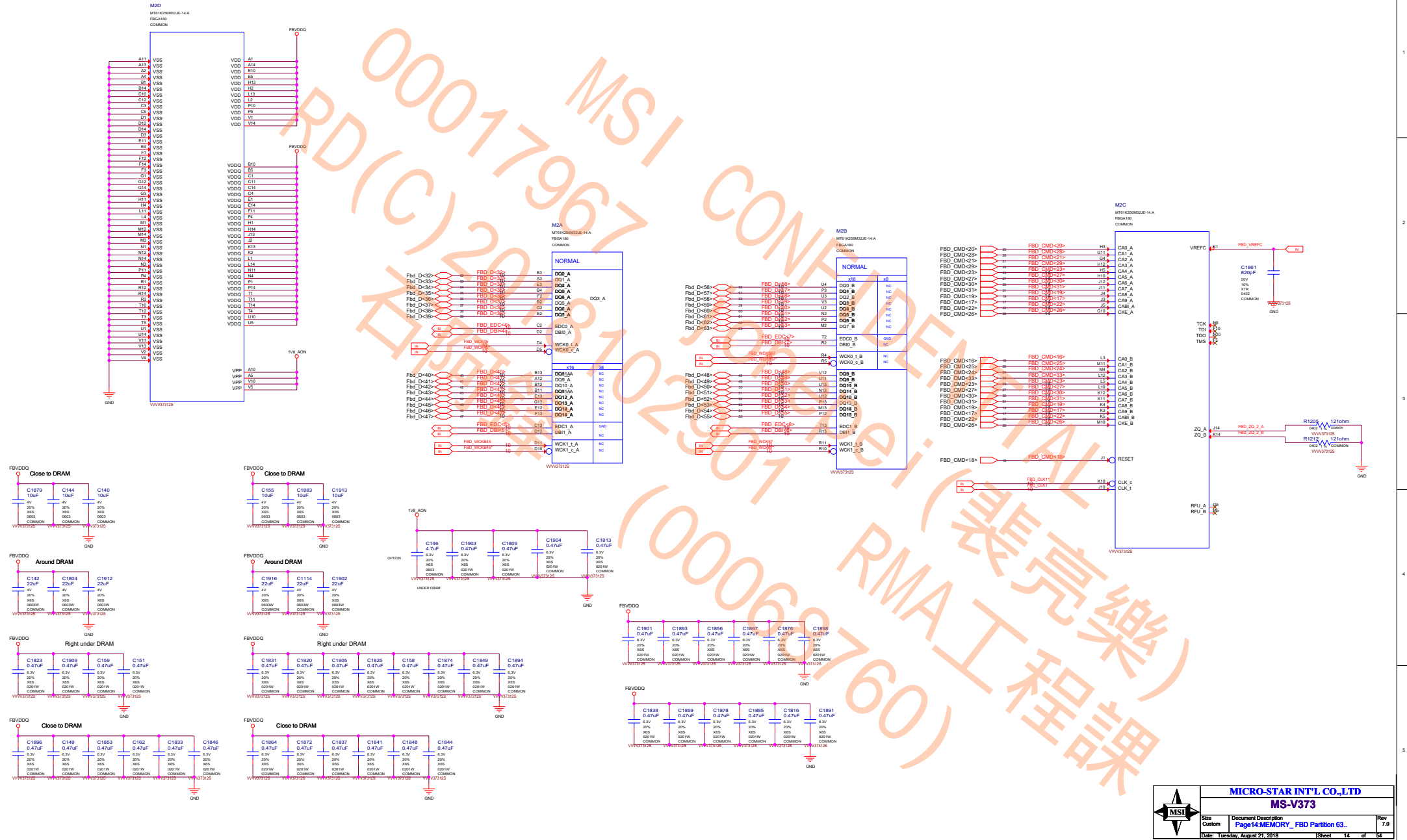




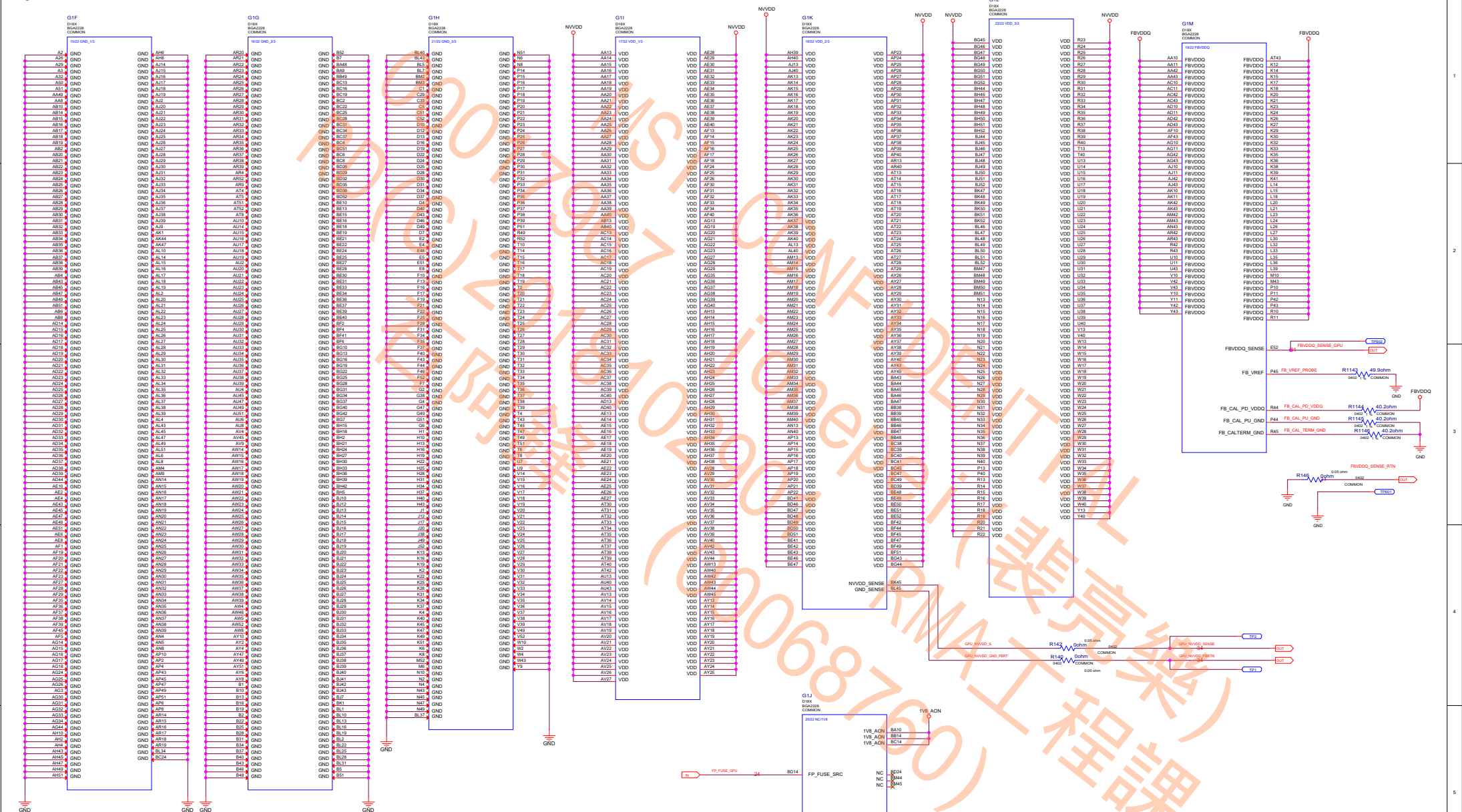










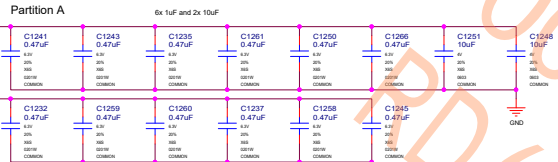




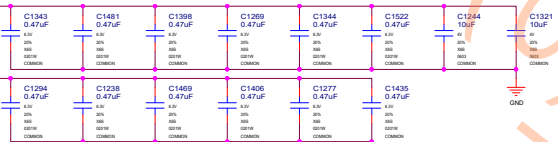
## NVVDD

## FBVDDQ

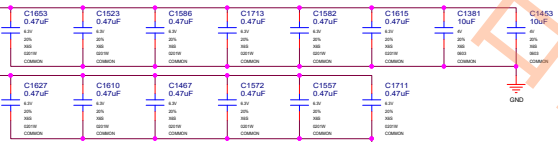
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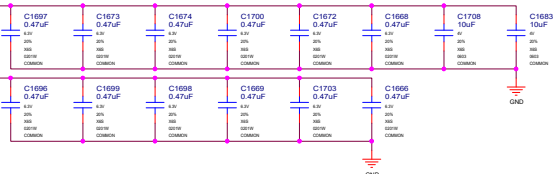
## Partition B



## Partition C



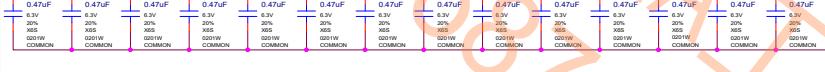
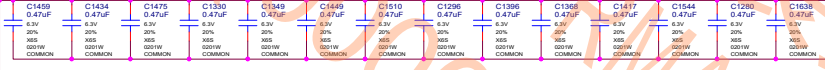
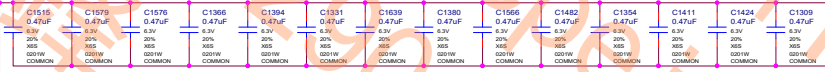
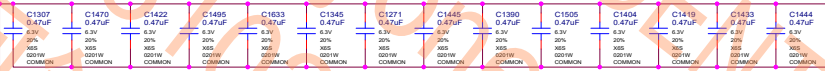
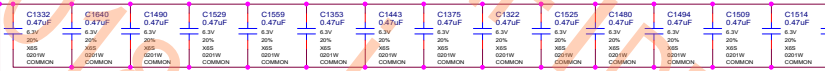
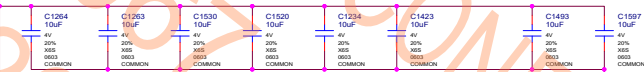
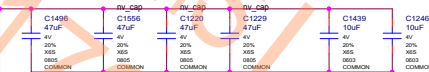
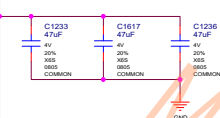
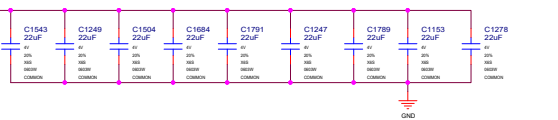
## Partition D



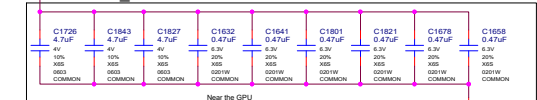
Place Close to GPU



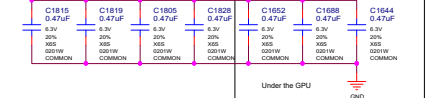
Place Close to GPU

032-0532-000  
X85  
0805

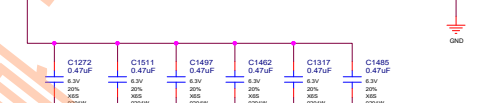
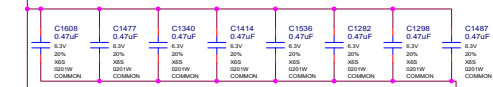
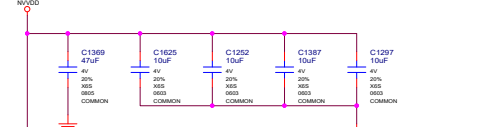
## 1V8 AON

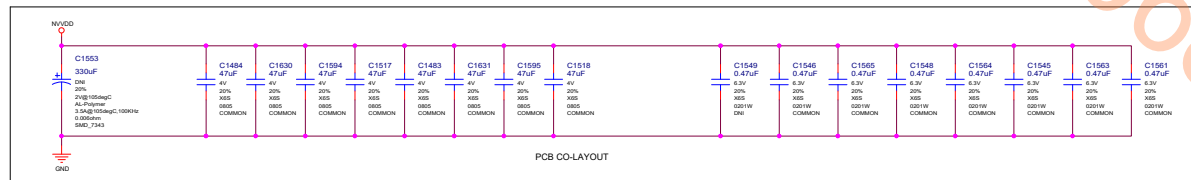
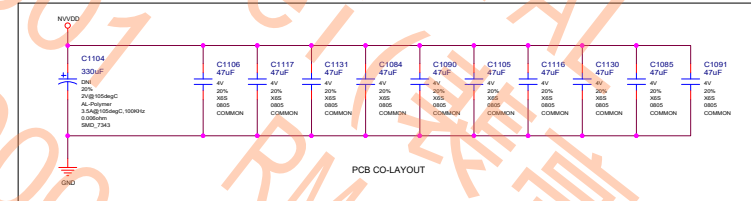
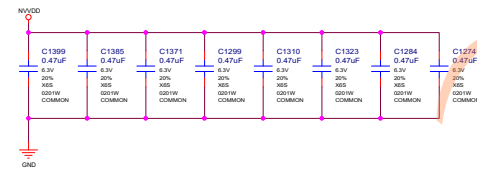
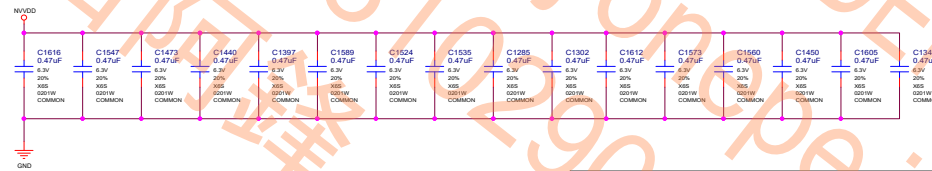
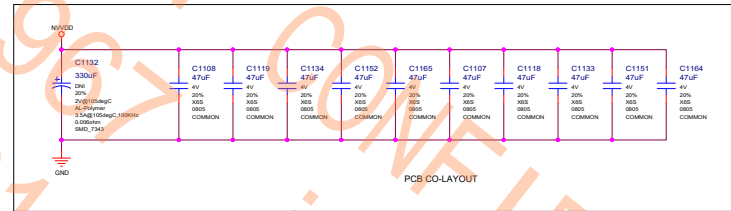
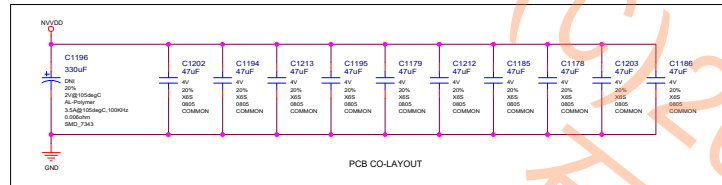
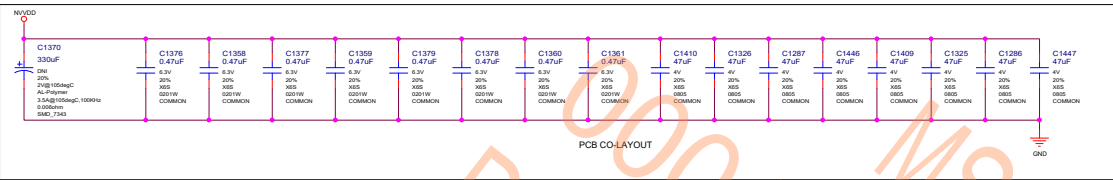


## 1V8 AON

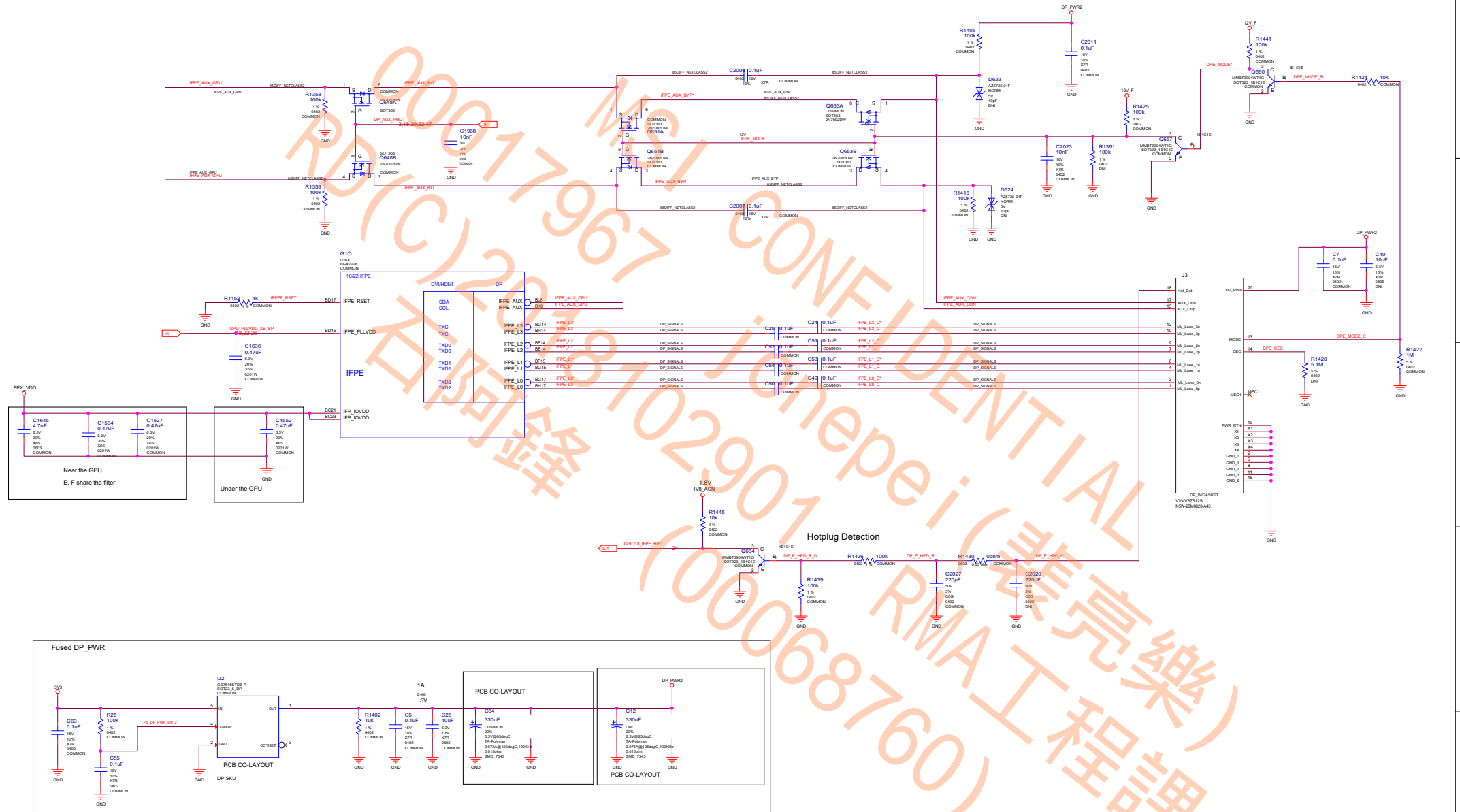


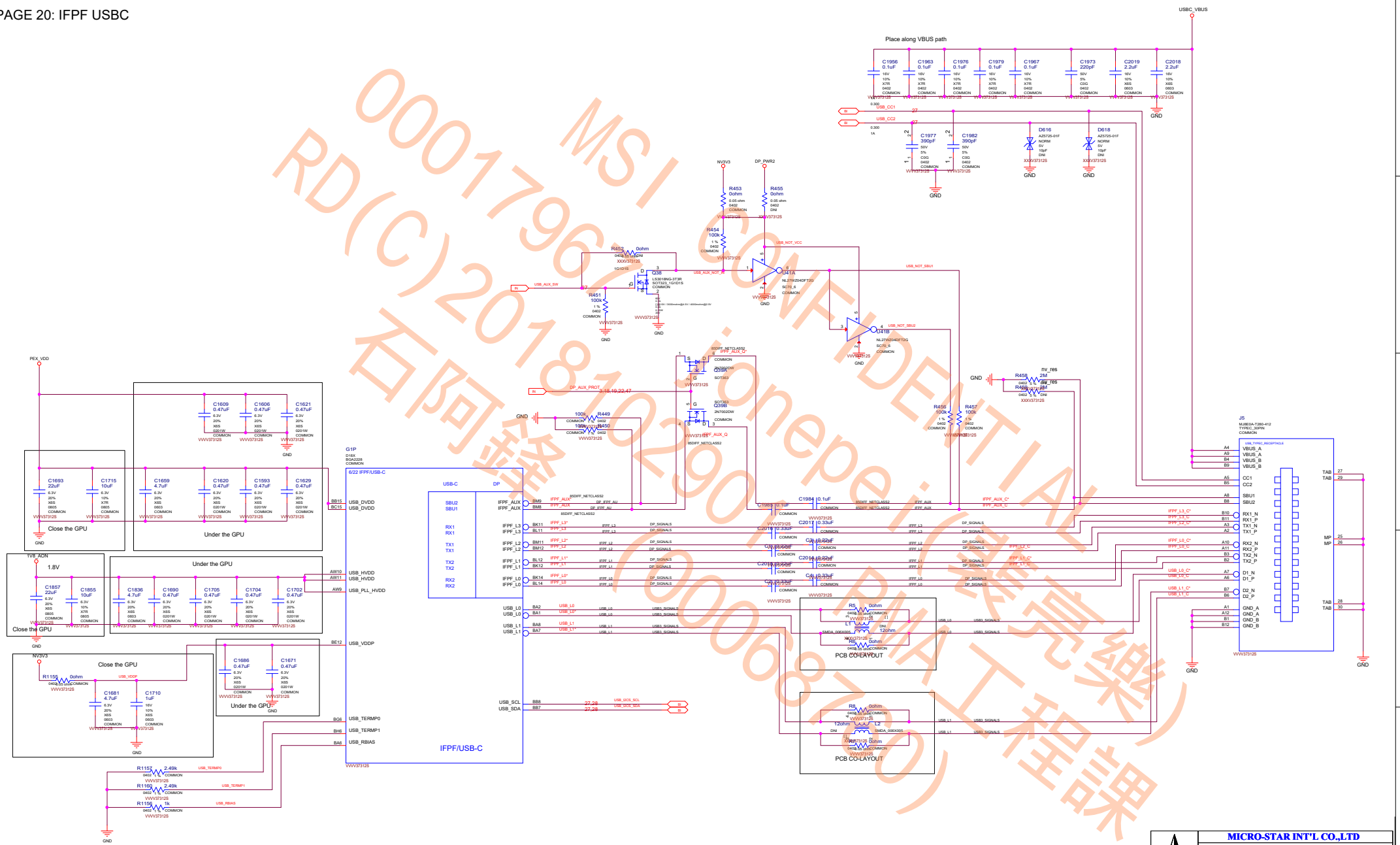
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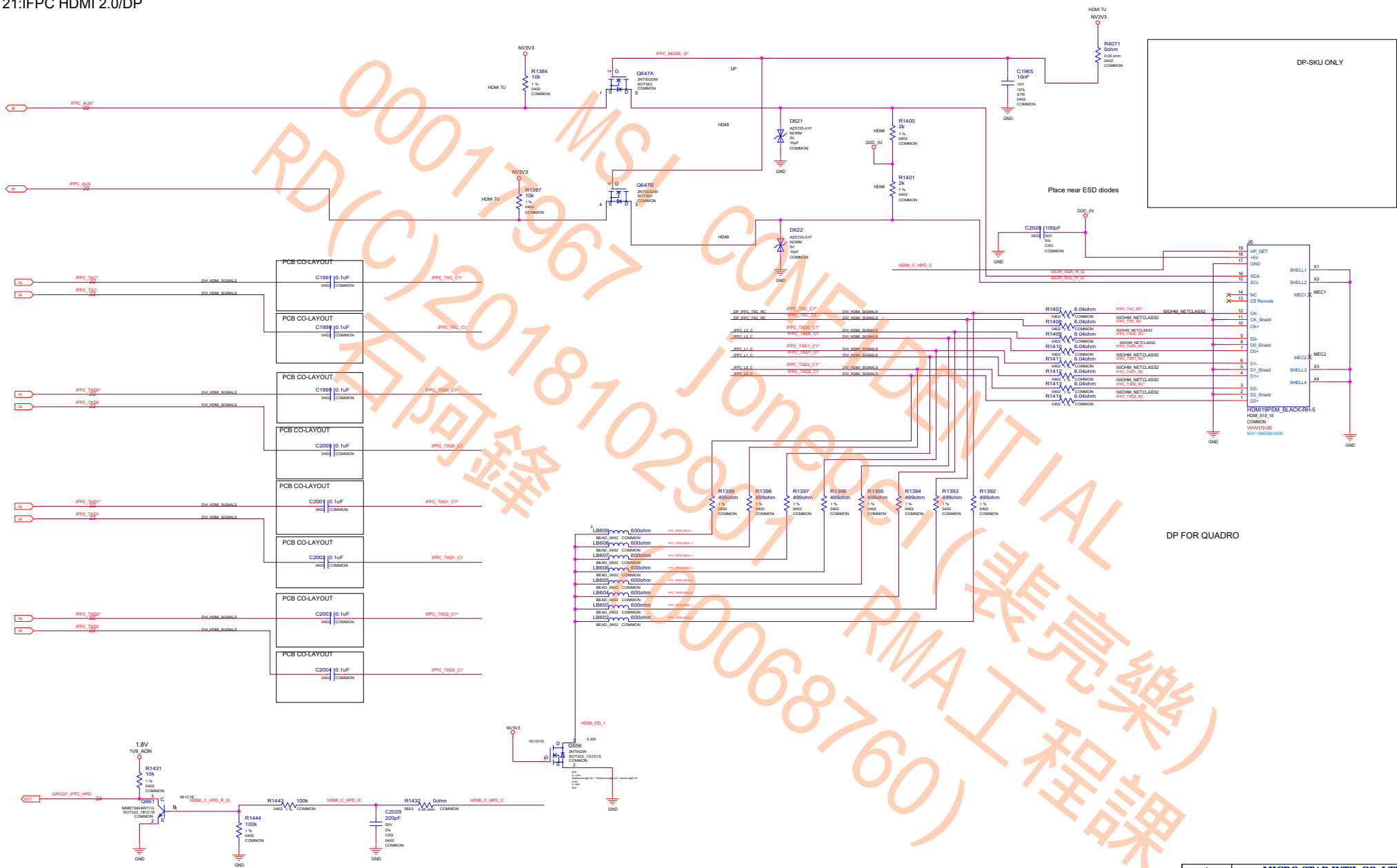
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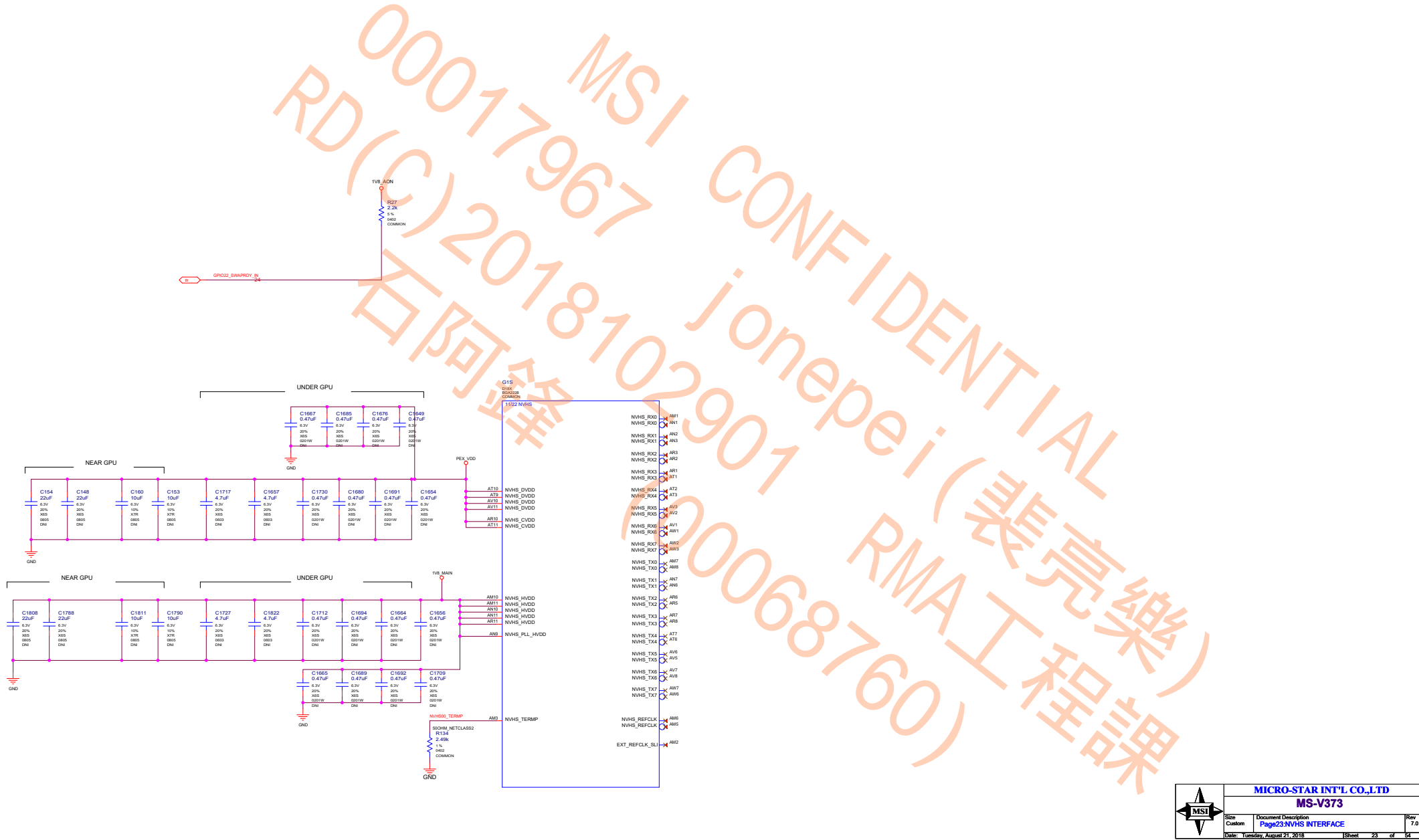














H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

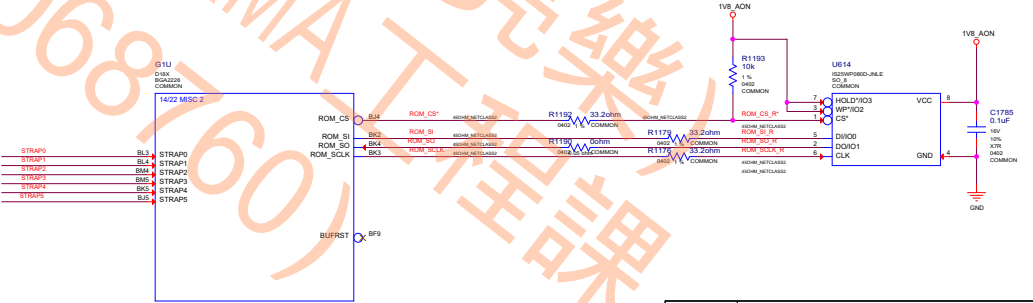
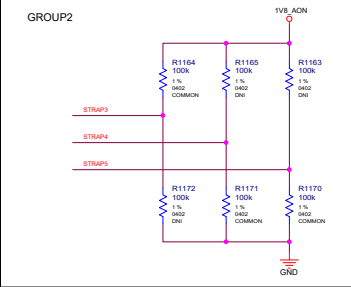
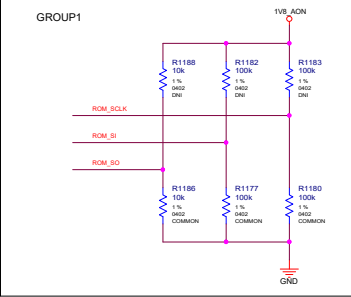
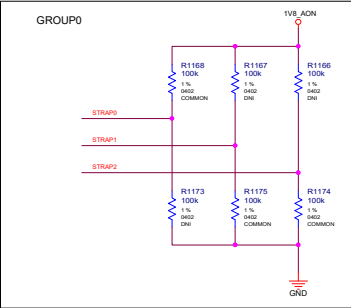
DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	0
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

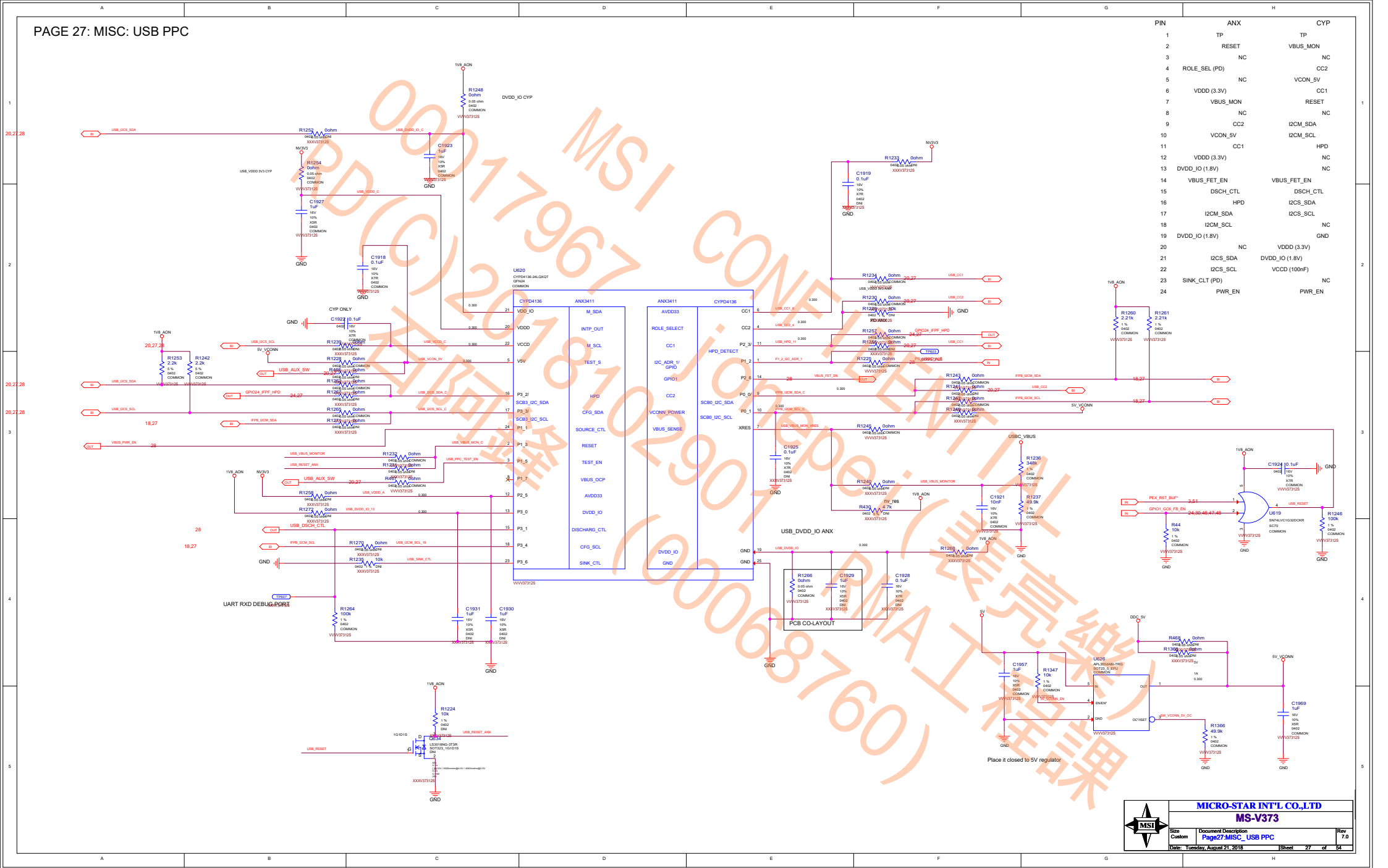
- 1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

Default

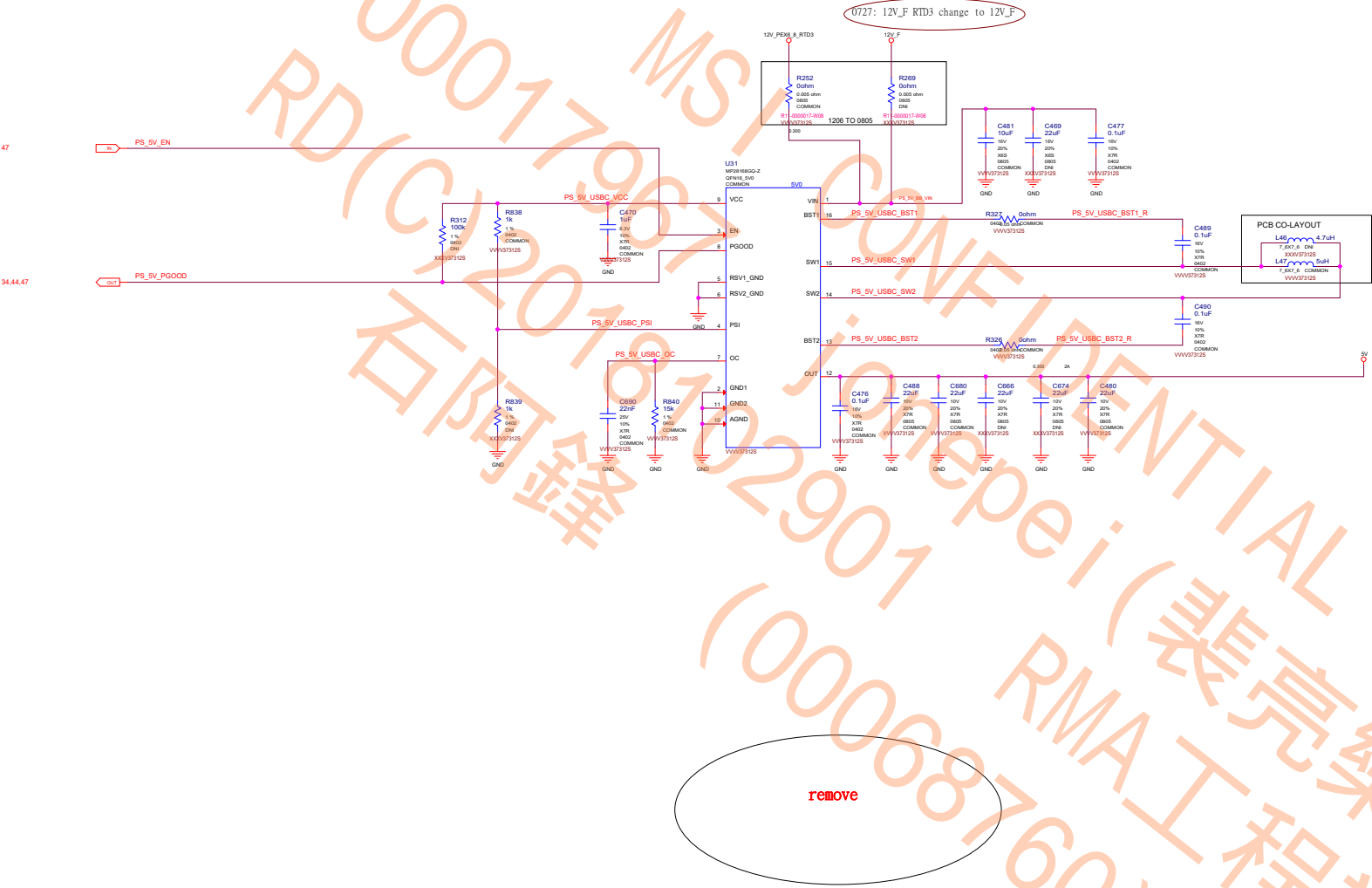
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



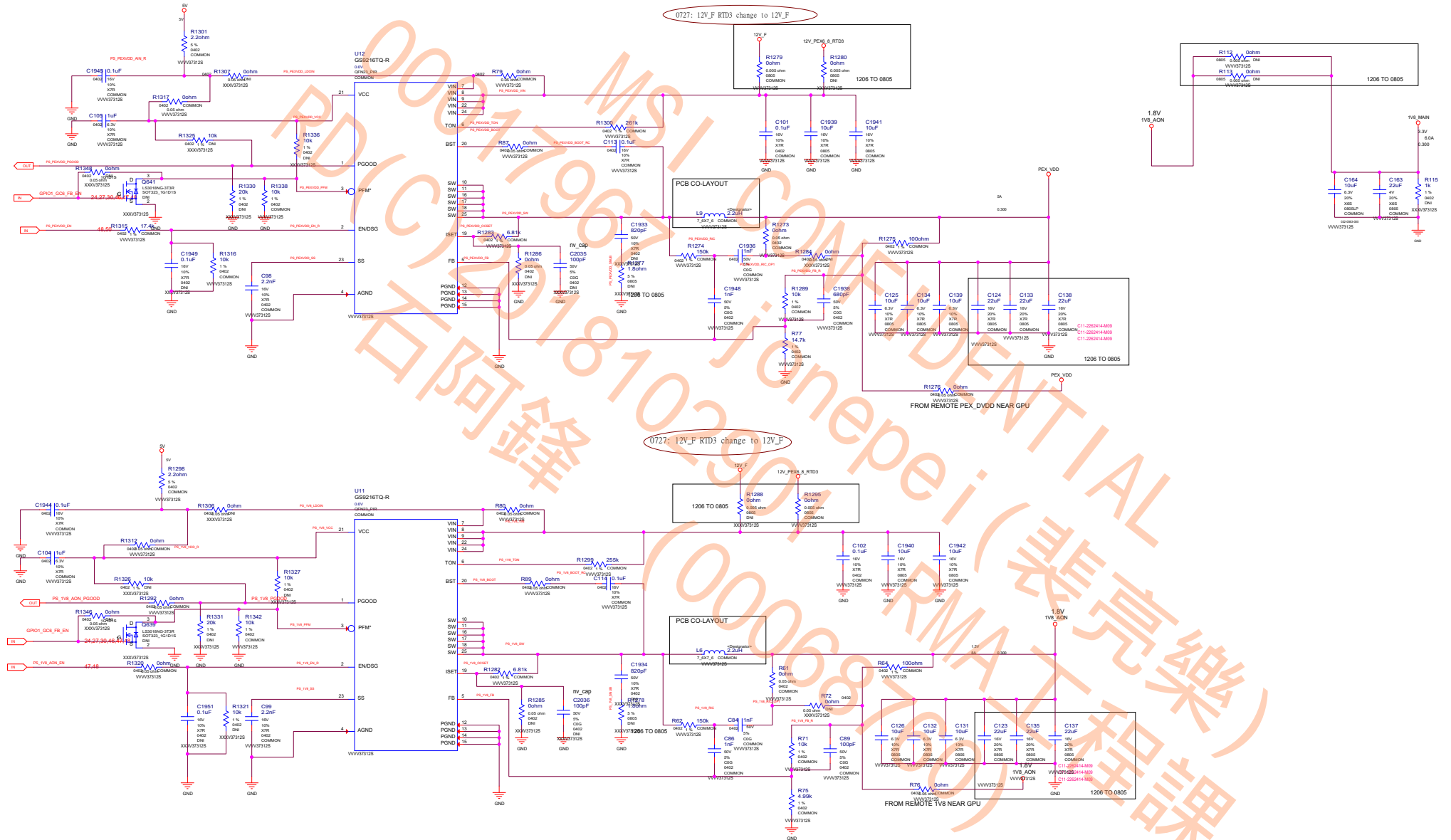













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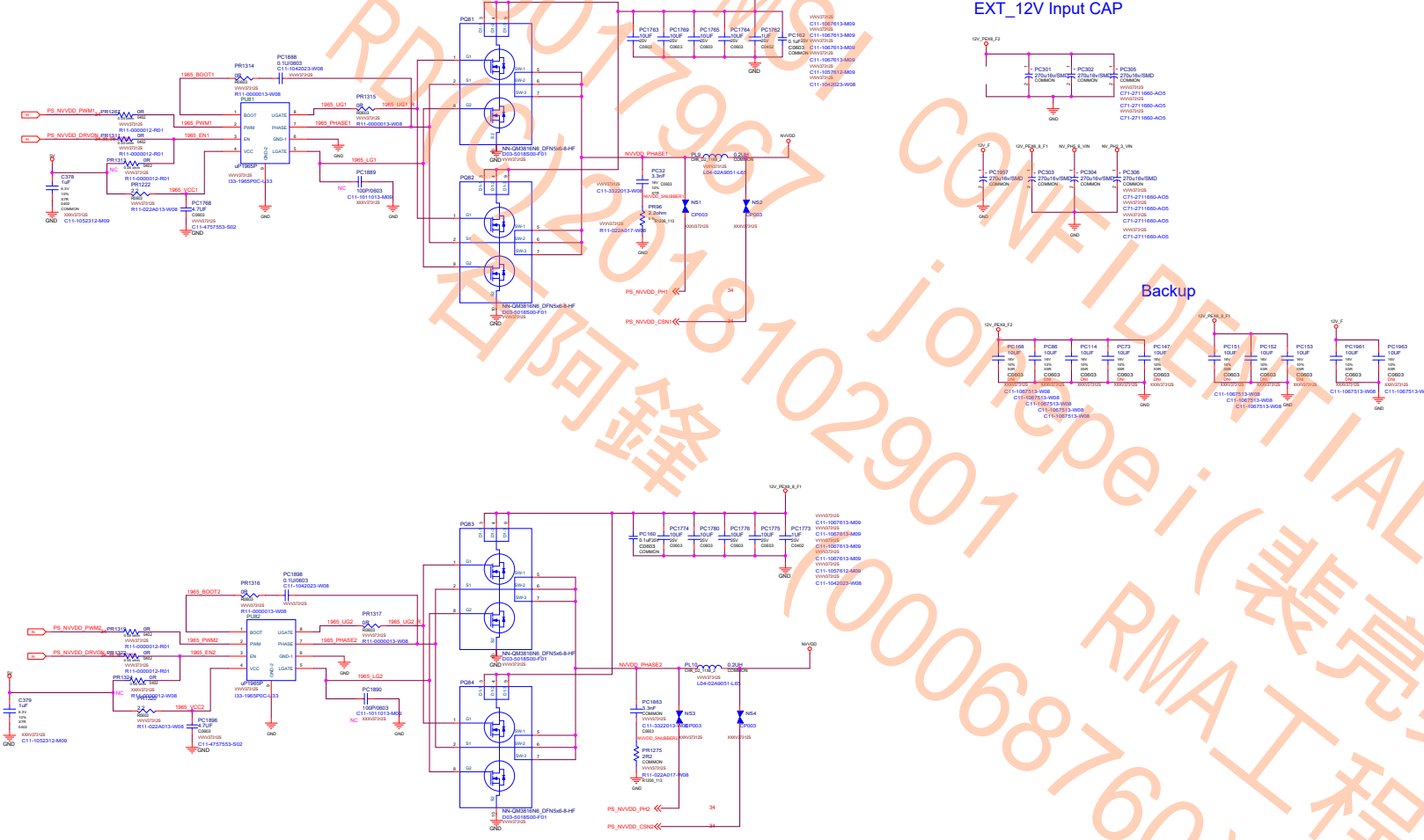


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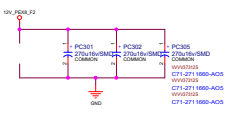
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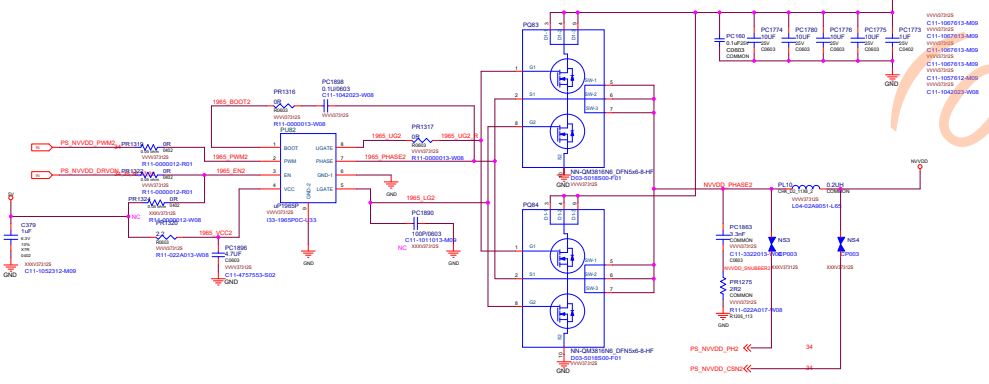
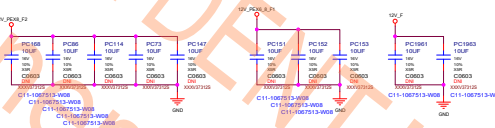


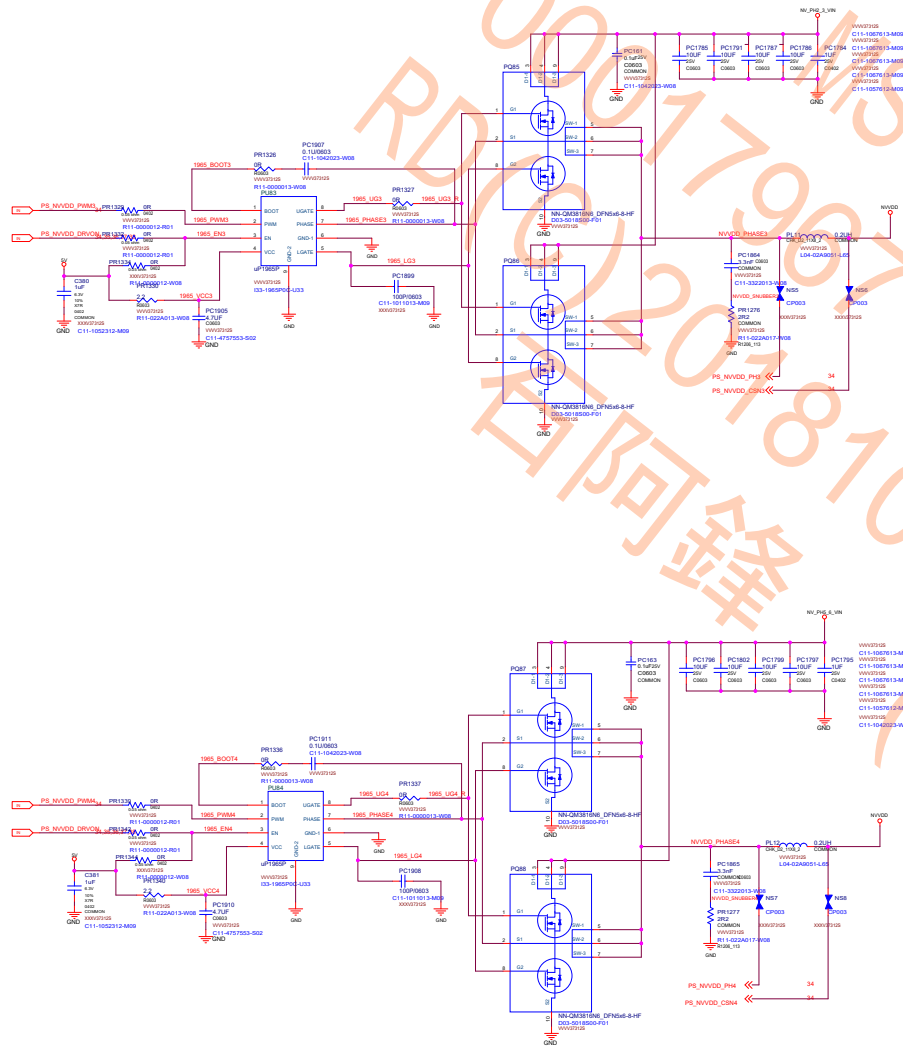


EXT\_12V Input CAP



Backup







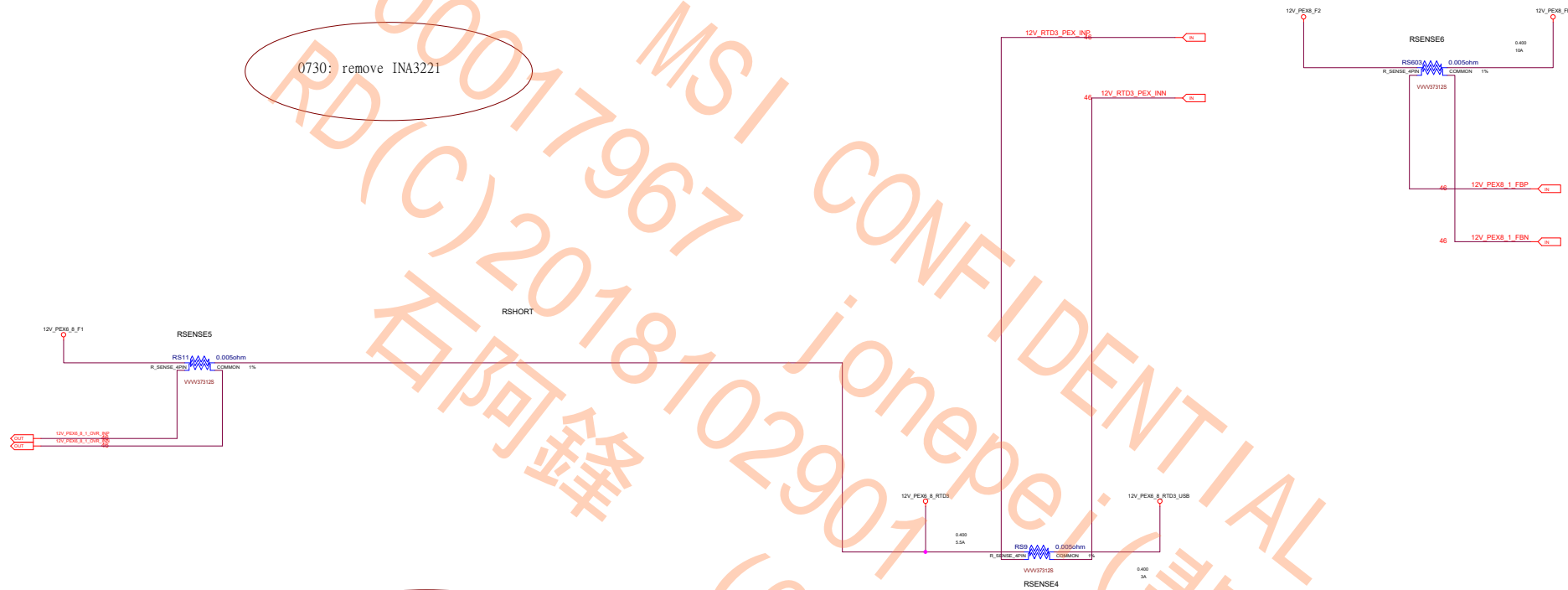




AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

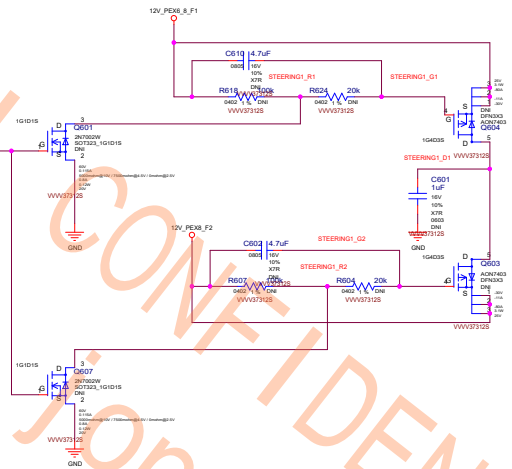
AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove

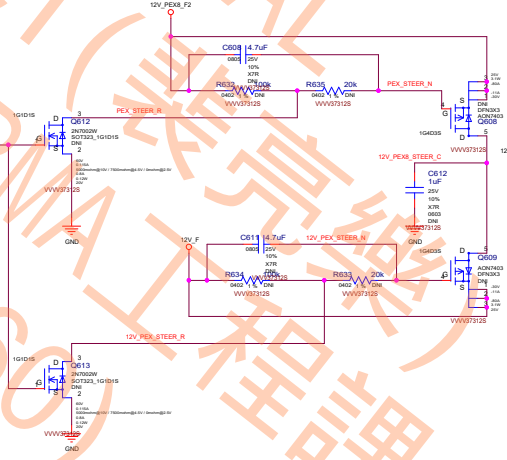




12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



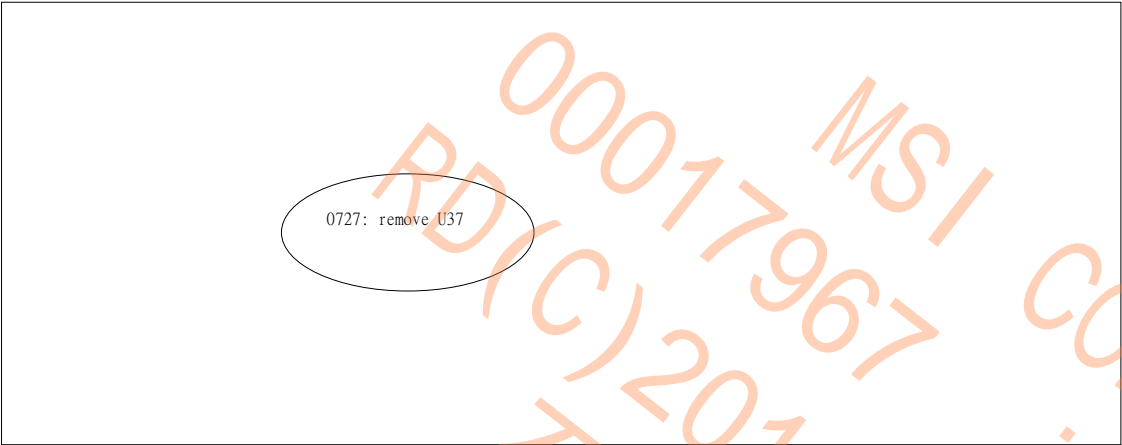
12V CURRENT STEERING (UNDER POWER BOOT):  
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



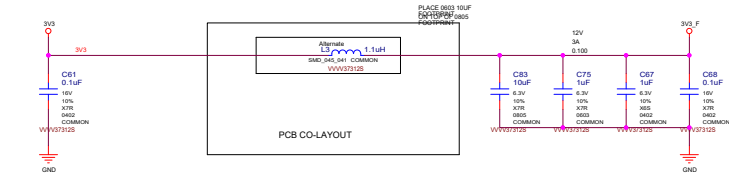
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石阿鋒 (00068760)

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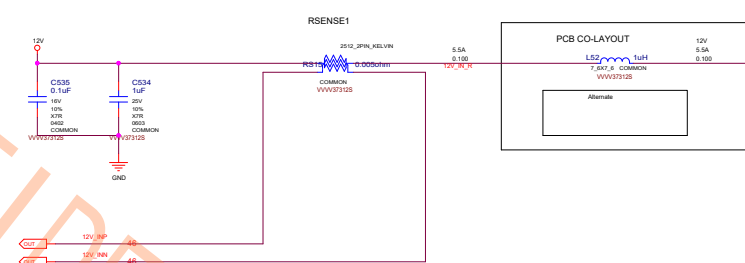




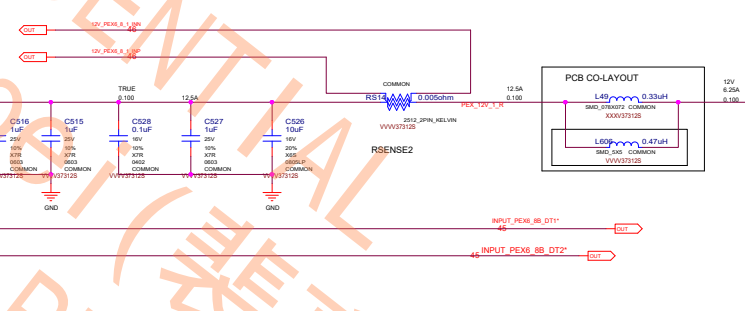
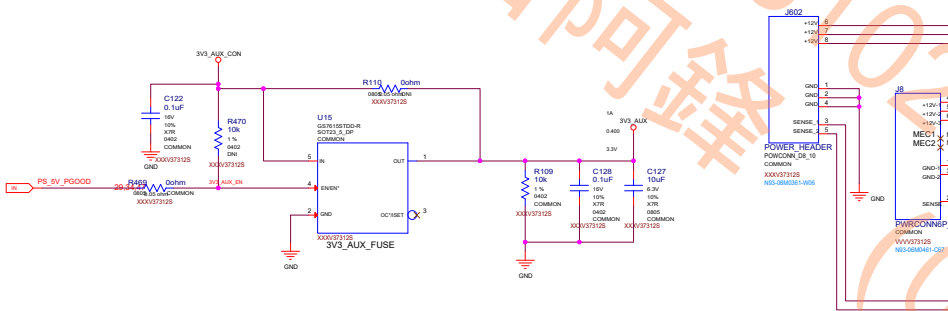
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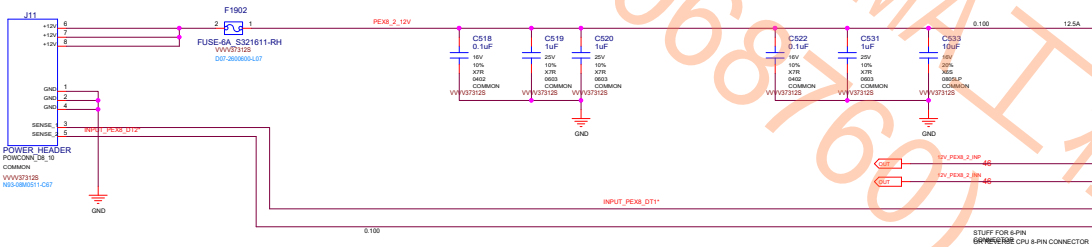
PEX\_12V INPUT - 66W



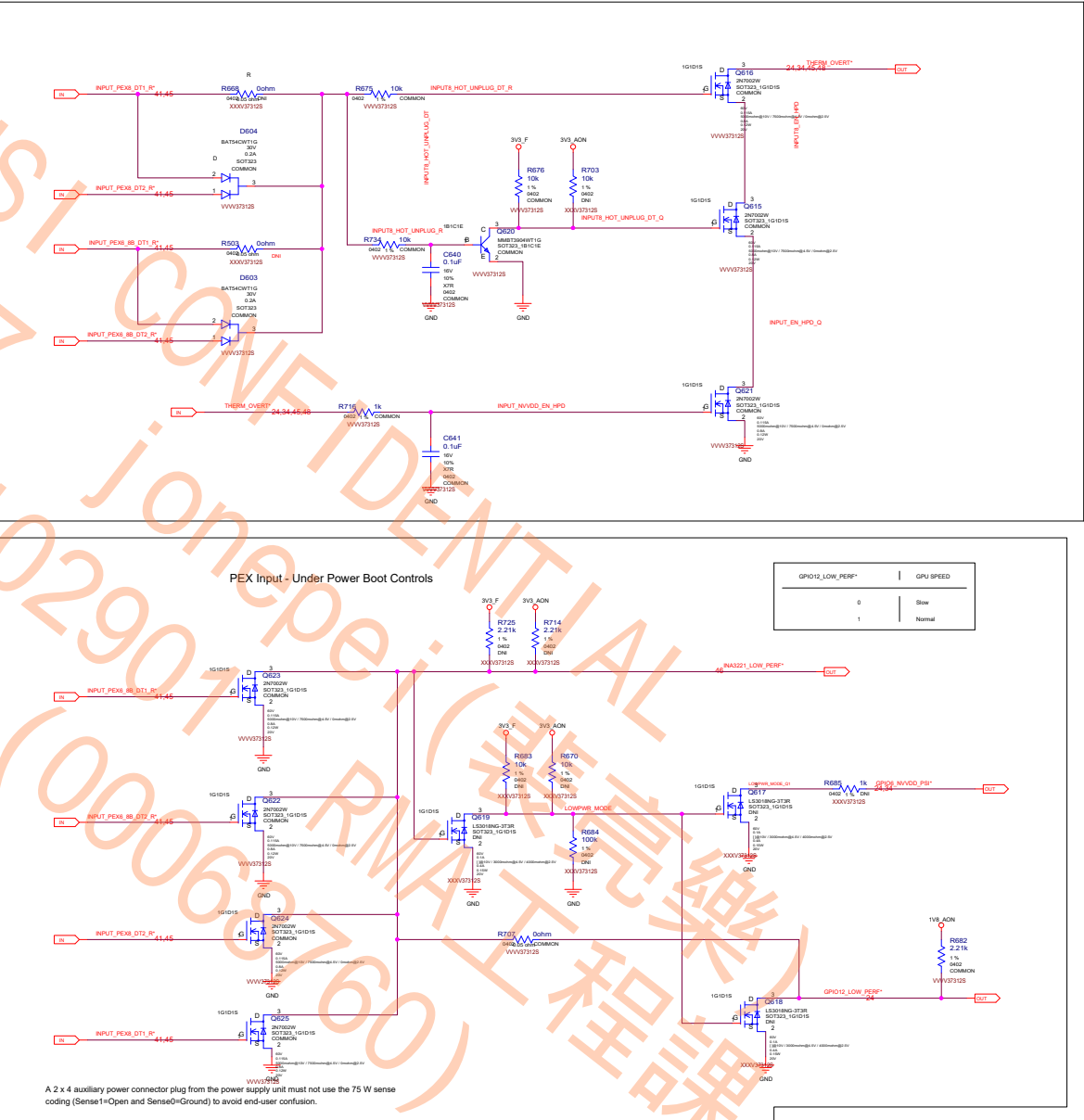
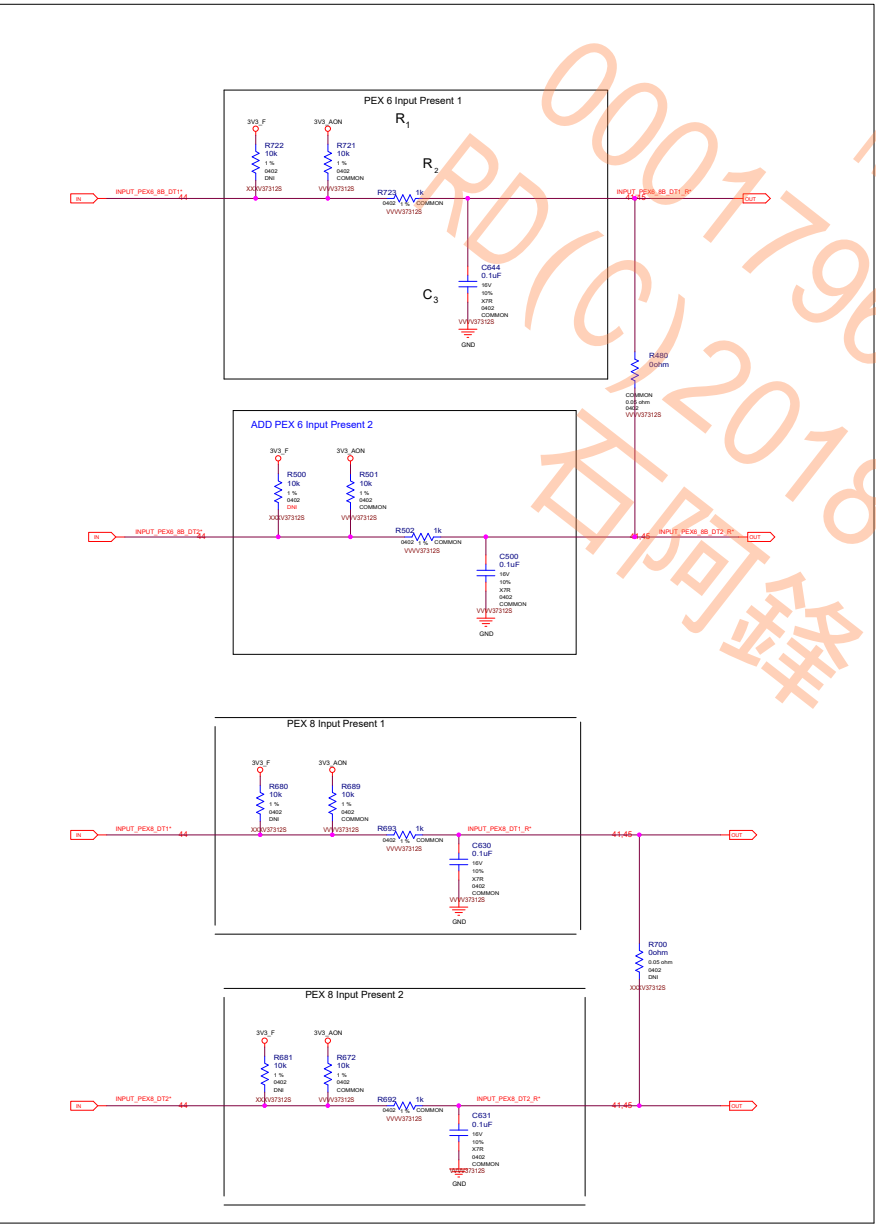
PEX6 INPUT 1 - 2x3 PCIE CON 75W



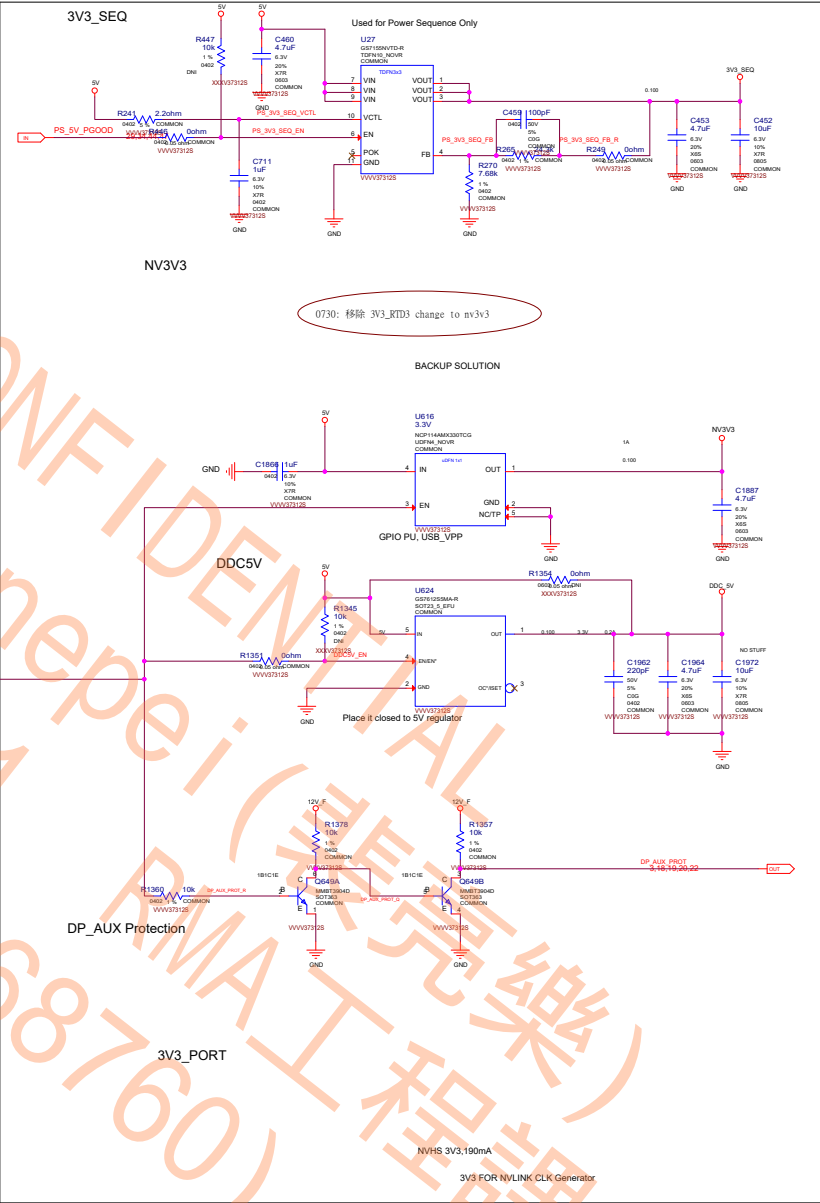
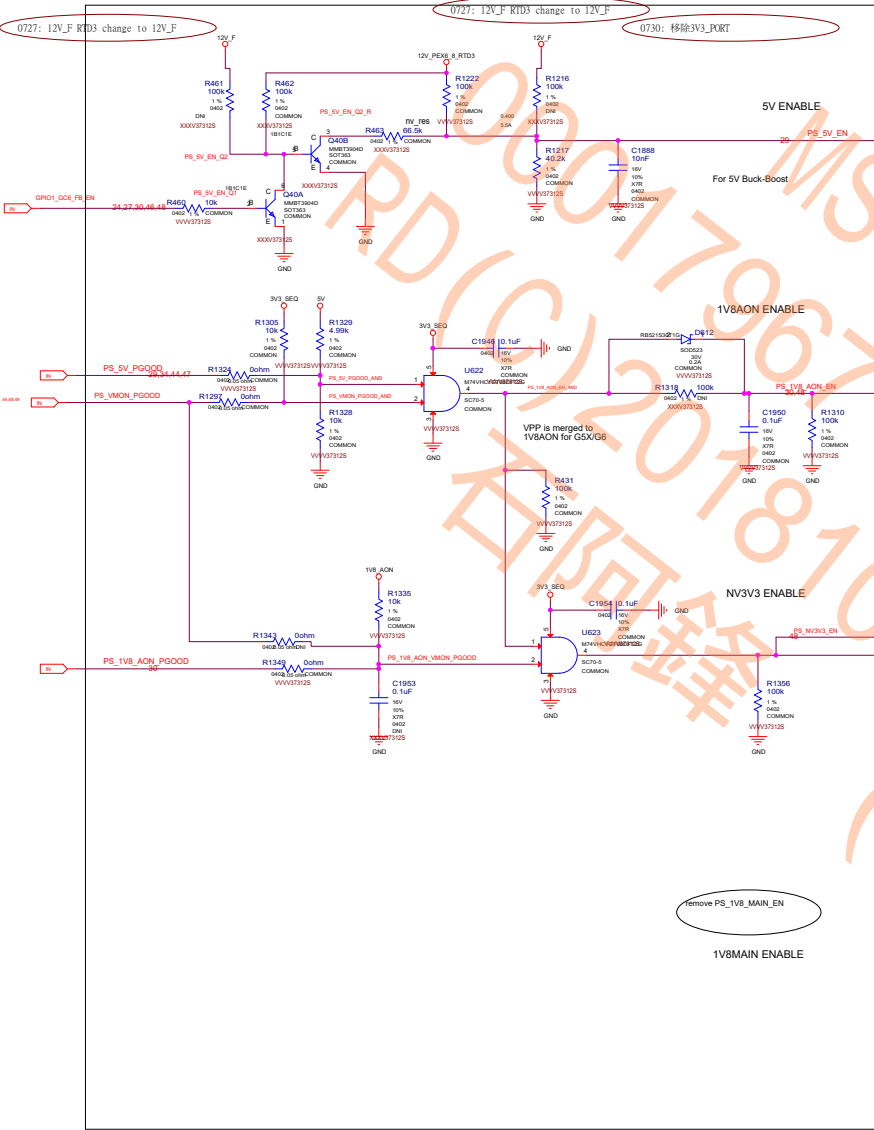
PLACE ON NORTH SIDE

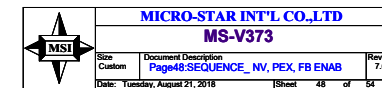
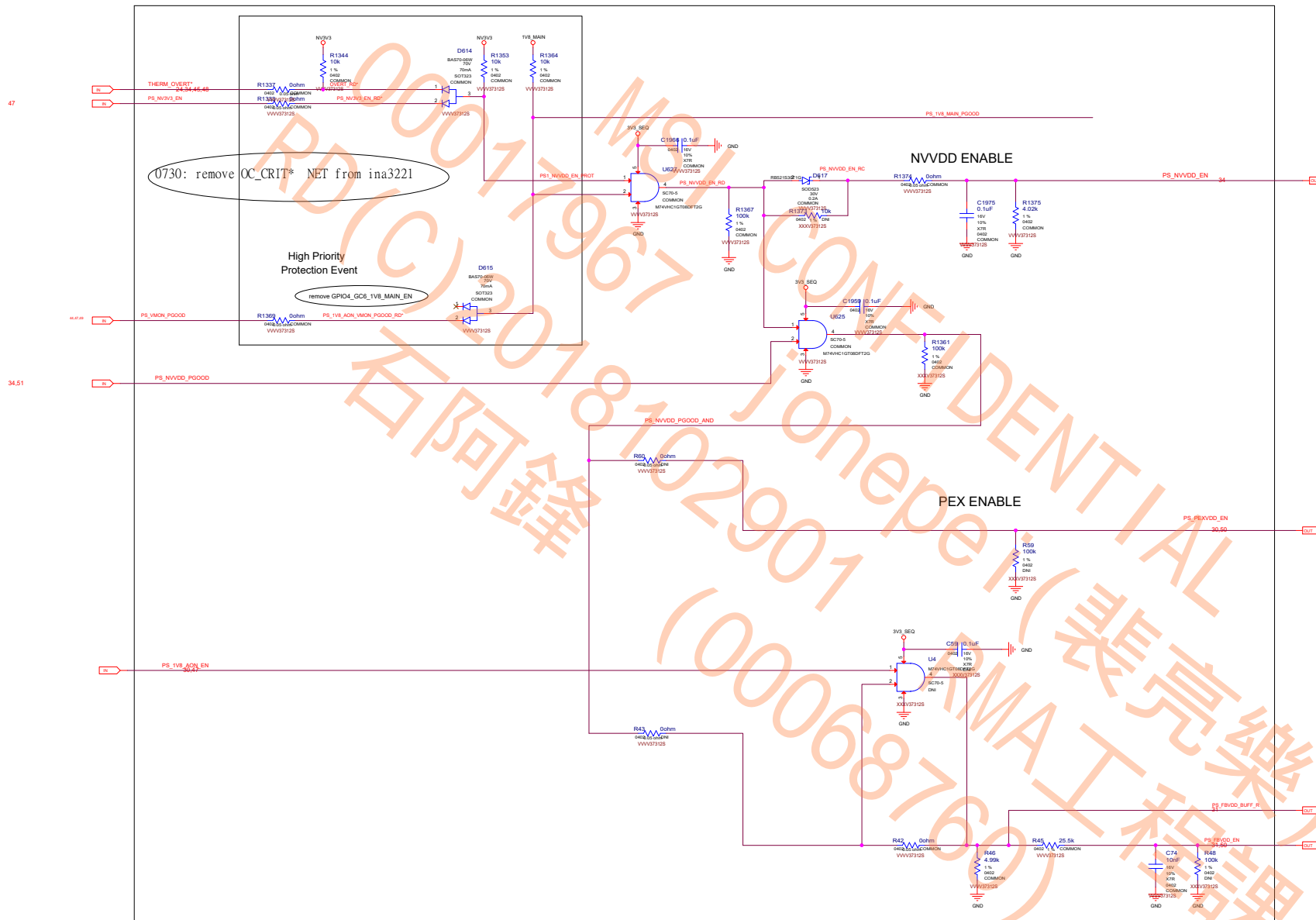


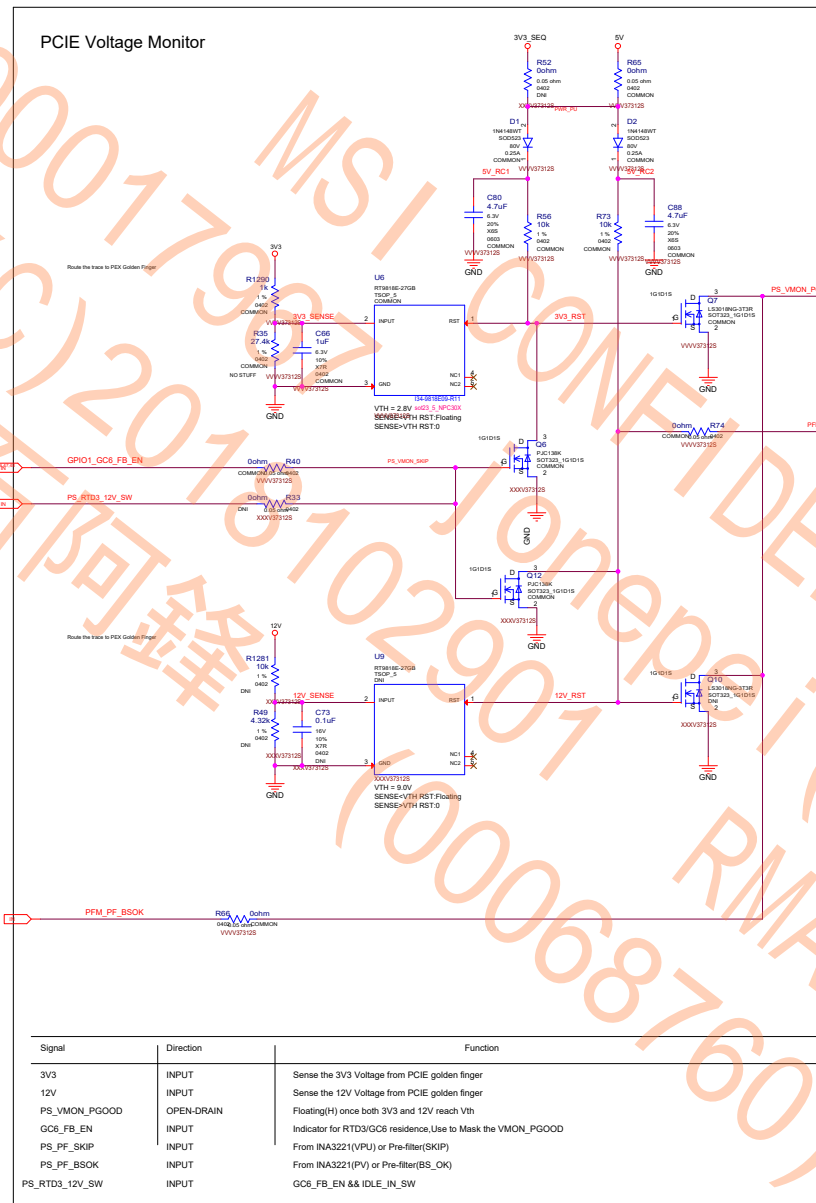
PEX8 INPUT 2 - 2x4 PCIE CON 150W











## BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

## Power Supply

INA3221:3V3\_SEQ

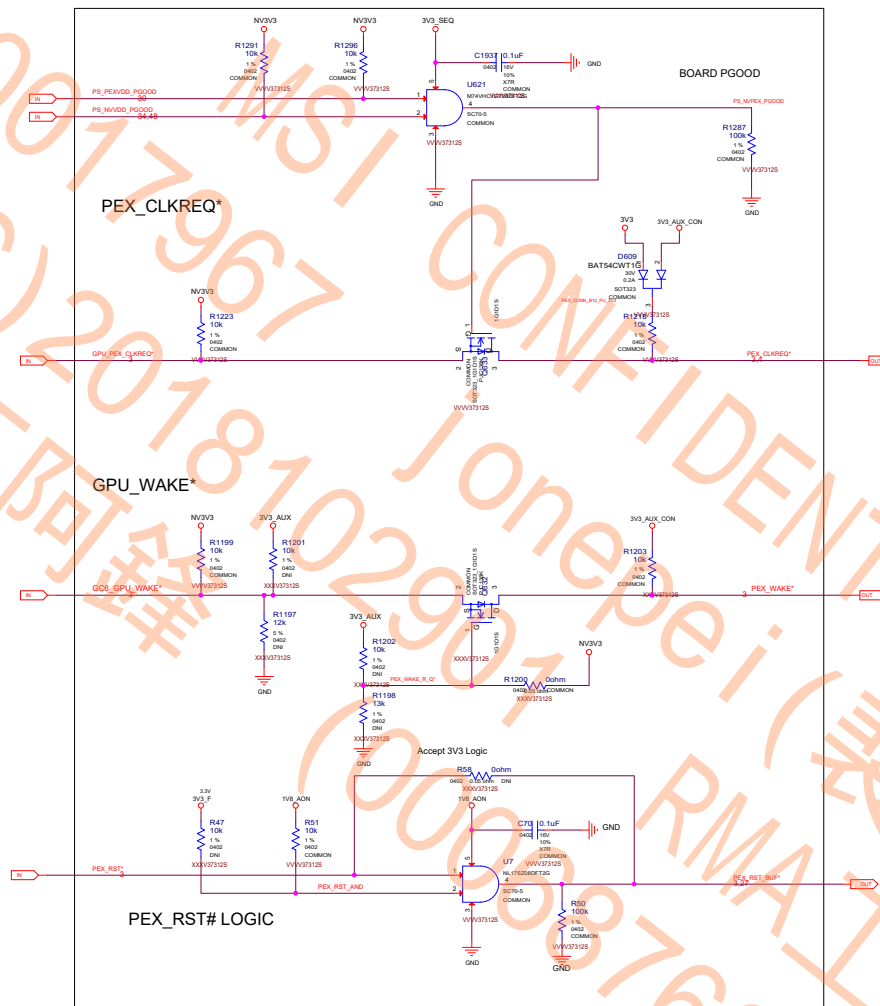
Pre\_Filter(ADC\_MUX):3V3(PEX)

## Dual Pre-Filter case:

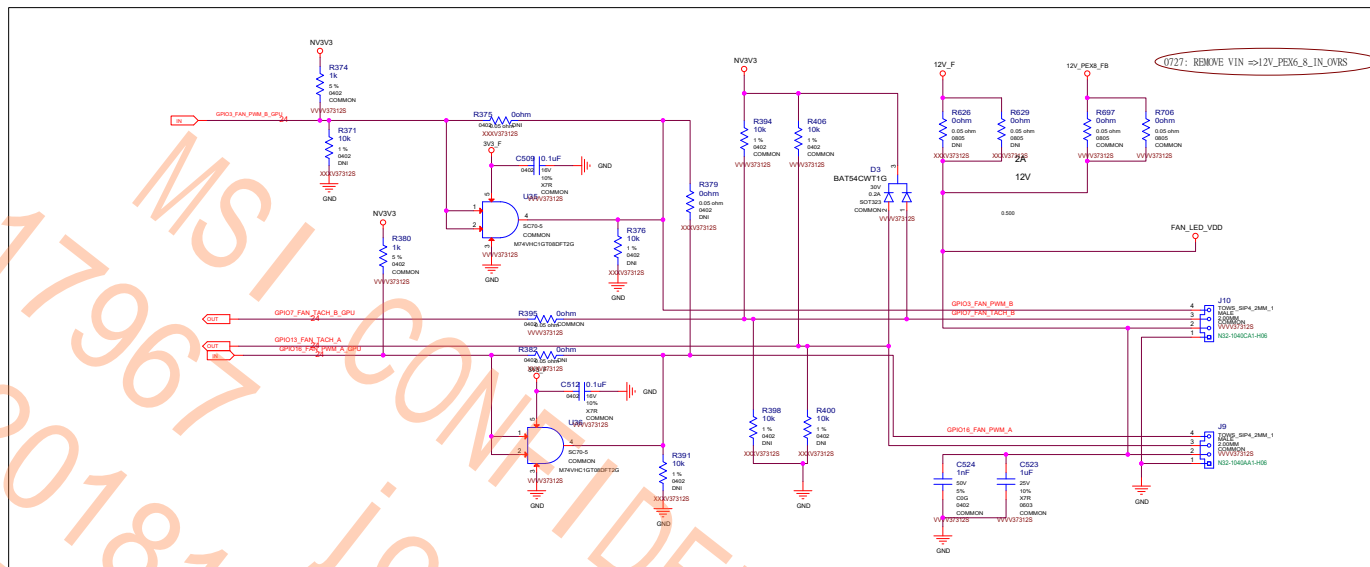
Only use the Primary Pre-Filter to sense 3V3PEX  
and All Input 12Vs







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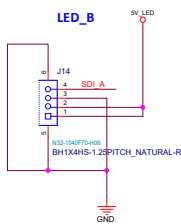
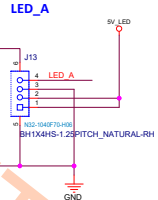
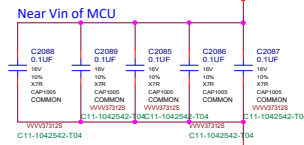
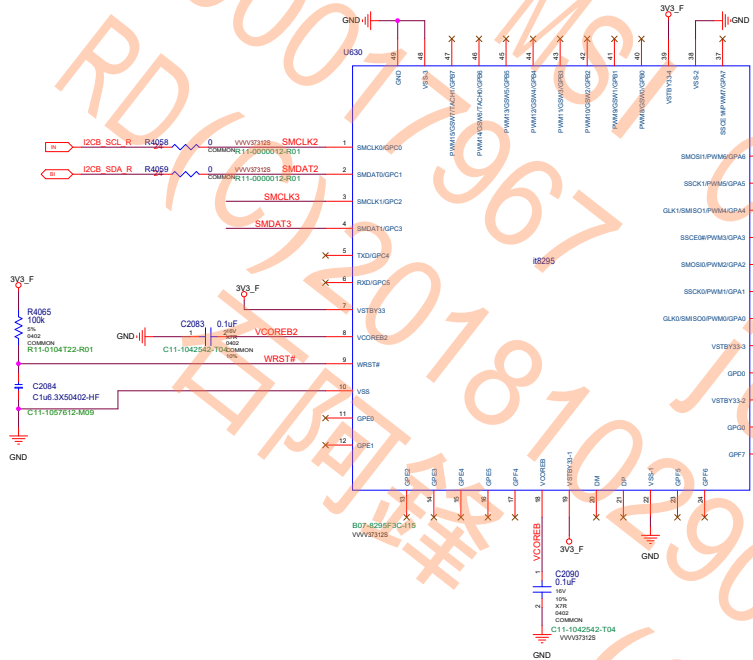
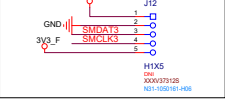


LED BOOST

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Firmware Programming

Debug



5V\_LED

